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A HIGH PERFORMANCE 128 BIT MAC USING PARALLEL PREFIX ADDERS

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Abstract: A design of high performance 64 bit Multiplier-and-Accumulator (MAC) is implemented in this paper. MAC unit is an inevitable many digital signal processing (DSP) applications involving multiplications and/or accumulations. MAC unit is used for high performance digital signal processing systems. The DSP applications include filtering, convolution, and inner products. Most of digital signal processing methods use nonlinear functions such as discrete cosine transform (DCT) or discrete wavelet transforms (DWT). Because they are basically accomplished by repetitive application of multiplication and addition, the speed of the multiplication and addition arithmetic determines the execution speed and performance of the entire calculation. This Paper presents a design of Low Power and High Speed MAC unit with Modified Wallace Multiplier and Parallel Prefix Adder. Further we extent the proposed 64 bit MAC unit to a 128 bit MAC in the way of increase the computational capacity of digital signal processor.

Keywords: Modified Wallace multiplier, Parallel prefix adder, Kogge-Stone adder, Carry Select adder, Carry Save adder.

I. INTRODUCTION

Multiplier-and-Accumulate (MAC) unit is associate inevitable half in many digital signal method (DSP) applications involving multiplications and/or accumulations. Water proof unit is utilized for prime performance digital signal method systems. The DSP applications embrace filtering, convolution, and inner merchandise. Most of digital signal method ways use nonlinear functions like separate mathematical function transform(DCT) or separate riffle transform(DWT). as a results of they're primarily accomplished by repetitive application of multiplication and addition, the speed of the multiplication and addition arithmetic determines the fastness and performance of the total calculation. Multiplication-and-accumulate (MAC) operations unit typical for digital filters. Therefore, the usefulness of the waterproof unit permits high-speed filtering and totally different method typical for DSP applications. Since the waterproof unit operates absolutely freelance of the Central method unit (CPU), it'll technique data severally and thereby reduce hardware load. The appliance like optical communication systems that depends on DSP, want terribly fast method of huge amount of digital data. the fast Fourier retread (FFT) jointly wants addition and multiplication. Sixty four bit can handle larger bits and have lots of memory. a water-proof unit consists of a number associated associate degree accumulator containing the full of the previous consecutive merchandise. The waterproof inputs unit obtained from the memory location and given to the number block.

1.1 MAC operation:

In computing, significantly in DSP applications, the multiply–accumulate operation might be a standard step that computes the merchandise of two numbers associated adds that product to AN accumulator. The hardware unit that performs the operation is known as a multiplier–accumulator, or waterproof unit. The operation itself is in addition typically observed as a water-proof or a water-proof operation. The waterproof operation modifies associate accumulator a:

$$a \leftarrow a + (b \times c) \quad \ldots\ldots \quad [1]$$

The mackintosh operation is that the key operation not alone in DSP applications but collectively in multimedia IP and varied completely different applications. As mentioned on prime of, mackintosh unit contains variety, adder and register/accumulator. during this paper, we tend to tend to used sixty four bit modified Wallace variety. The mackintosh inputs unit obtained from the memory location and given to the quantity block. this could be useful in sixty four bit digital signal processor. The inputs that's being fed from the memory location is sixty four bit. once the input is given to the quantity it starts computing worth for the given 2-64 bit inputs and thence the output ar about to be 128 bits. the quantity output is given as a result of the input to adder that performs addition. The perform of the mackintosh unit is given by the following equation:

$F = \sum P_i Q_i$

The basic architecture of MAC unit is as shown below.

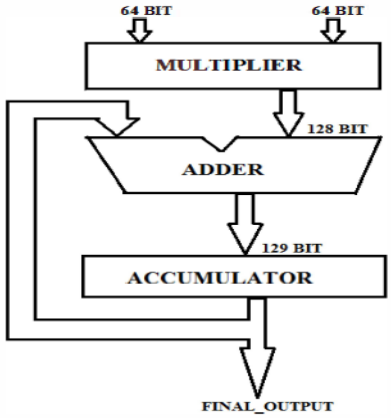


Figure 1: Basic Architecture of 64 bit MAC unit

The output of adder is 129 bit i.e. one bit is for the carry (128bits+ one bit). Then, the output is given to the register.

The register used during this vogue is Parallel-in-Parallel-out (PIPO). Since the bits ar huge and in addition adder produces all the output values in parallel, PIPO register is used where the input bits area unit taken in parallel and output is taken in parallel. The output of the register is taken out or fed back along of the input to the adder.

A. Adders:

Addition is that the foremost typical and typically used mathematical process on chip and digital signal processor, significantly digital computers. in addition it's building block for synthesize all operation. Therefore, concerning the economical implementation of Associate in nursing arithmetic unit, the binary adder structure becomes a very crucial hardware unit. In any book on portable computer arithmetic, someone look that there exits associate oversized variety utterly totally {different|completely different} circuit arithmetic with different performance characteristics and wide used in follow. although many researches handling binary adder structure area unit done, the studies supported the performance analysis unit of measurement only few.

In this project, chemical analysis of the classified binary adder structures area unit given. Among an outsized type of the adders, verilog code for ripple carry, carry select and carry look ahead to emphasise the common performance properties belong to their categories at intervals the subsequent section, we've got a bent to gave temporary description of the studied adders style. With connectedness the line delay time and house quality, the binary adder style is characterised into four primary classes and very advanced for the high bit lengths of the operands. the primary class consists of the very slow ripple carry adder with the littlest house. at intervals the second class carry select and carry skip adders with multiple levels have little house requirements and short end computation times. From the third class carry look ahead adder and therefore the fourth class, the parallel prefix adder represent fastest addition schemes with the largest house complexities. the ultimate step in finishing the multiplication procedure is to feature the final word terms at intervals the ultimate adder. this will be normally named as "Vector-merging" adder. the choice of the final word adder depends on the structure of the buildup array Following may well be a listing of quick adders that area unit normally used.

Carry select adder:

Carry select adder depends on anticipation of output carry for two getable values of input carry. Once the vital value of the incoming carry is believed, the proper result's merely elect with a simple device stage. Carry select adder square measure typically implemented in two alternative ways in which

1) Linear carry select adder
2) Square-root carry select adder.

Consider the block of adders, that's adding bits k to k+3. instead of waiting on the arrival of the output carry of bit k-1, every the zero and one probability is analyzed. A device square measure typically used to select either of the results once Co, k-1 settles. The hardware overhead of the carry select adder could be a any carry path and a device. A basic structure of linear carry select adder is shown in Figure a two.17.

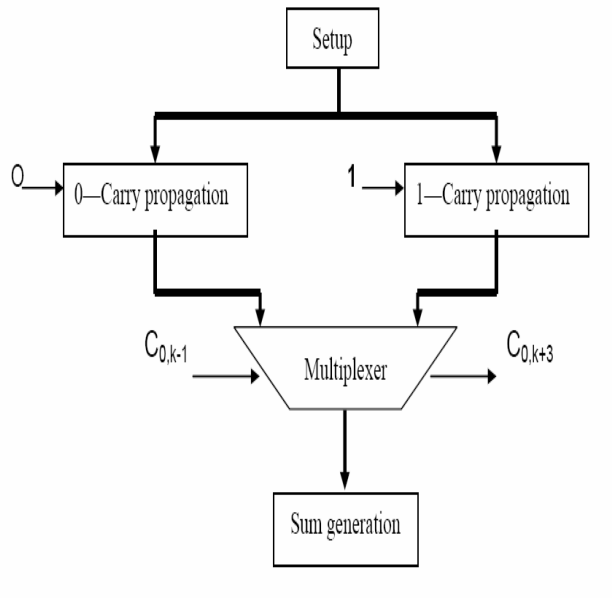


Figure 3 Carry select adder module

A full carry select adder is now built using a chain of equal-length adder stages, as in carry bypass adder. The propagation delay of N-bit adder with M-bit stages can be determined as follows

$$T_{add} = t_{setup} + Mt_{carry} + \lceil N/M \rceil t_{mux} + t_{sum}$$

The carry select adder can be optimized to reduce the delay of critical path by making the adder stages progressively longer than the previous ones. This architecture results in square root dependence and is called square root carry select adder.

Carry save adder

The carry save adder contains n full adders, computing one total and carries bit based totally mainly on the varied bits of the three input numbers. the whole total are calculated by shifting the carry sequence left by one place so appending a zero to most important little of the partial total sequence. presently the partial total sequence is superimposed with ripple carry unit resulting in n+ one bit value. The ripple carry unit refers to the tactic where the carryout of one stage is gulped up to the carry in of future stage. This technique is sustained whereas not adding any intermediate carry propagation. A typical eight bit carry save adder is shown at intervals the figure a combine of.19. Here we've an inclination to ar computing the full of two eight bit binary numbers, then eight zero.5 adders at the first stage instead of eight full adder. Therefore , carry save unit contains of eight zero.5 adders, each of that computes single total and carry bit based totally exclusively on the corresponding bits of the two input numbers. If x and y ar imagined to be two eight bit numbers then it produces the partial merchandise and carry as S and C severally.

$S_i = x_i \wedge y_i$
$C_i = x_i \& y_i$

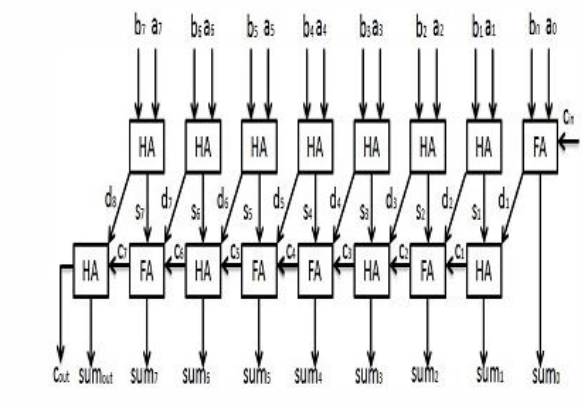


Figure 4 8-bit carry save adder

During the addition of 2 numbers employing a 0.5 adder, 2 ripple carry adder is employed. this can be due the very fact that ripple carry adder cannot figure a total bit while not looking forward to the previous carry bit to be created, and therefore the delay are adequate that of n full adders. but a carry-save adder produces all the output values in parallel, leading to the full computation time but ripple carry adders. therefore Parallel-In-Parallel-out (PIPO) is employed as Associate in Nursing accumulator within the ending.

Parallel prefix adders:

In the projected waterproof unit, kogge-stone adder is employed as a result of it's minimum spread out of one at every node (implies quicker performance) and low depth (less calculation time). therefore Kogge-stone contributes its blessings for top performance MAC unit.

1. Kogge-Stone Adder:

Kogge-Stone adder could be a parallel prefix kind carry-look-ahead adder. The Kogge-Stone adder was developed by Peter M. Kogge and Harold S. Stone that they printed it in 1973. Kogge-Stone prefix adder could be a quick adder style. Kogge-Stone adder has best performance in VLSI implementations.

The 2-bit and 32- bit Kogge- Stone adder figures shown below.

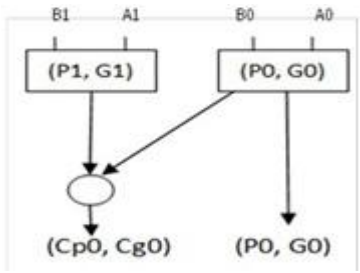


Figure.5 2-bit Kogge-Stone Adder

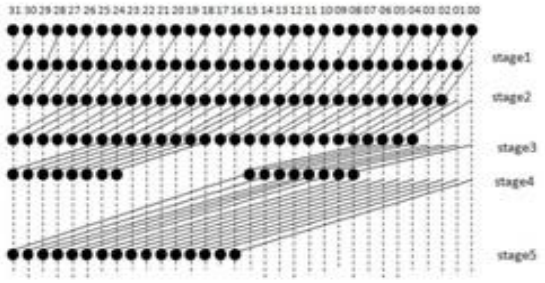


Figure.6 32-bit Kogge-Stone Adder

BRENT-KUNG ADDER

The Brent-Kung adder may be a parallel prefix adder. The goose-Kung adder was developed by Brent and Kung that they revealed in 1982. the amount of cells is calculated by victimisation 2(n-1)-Log2n .

- It has most logic depth.
- It has minimum space.

The 4-bit and thirty two bit Brent- Kung adder figures is shown below.

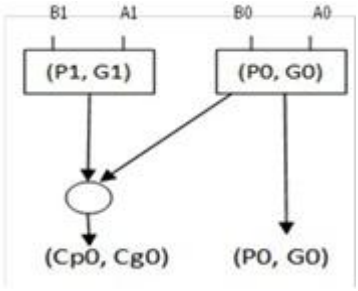
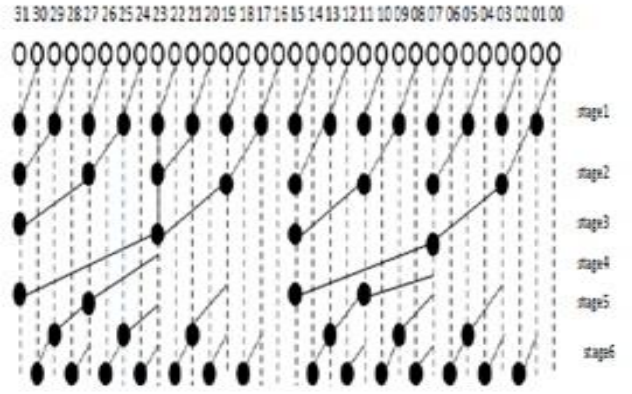


Figure.7 2-bit Brent-kung adder



Figur.8 32-bit Brent-kung adder

B. Modified Wallace Multiplier

Multiplication is one in each of the foremost typically used operations inside the arithmetic. Multipliers supported Wallace reduction tree supply degree area-efficient strategy for prime speed multiplication. style of modifications ar planned inside the literature to optimize the planet of the Wallace multiplier. A modified Wallace number (MWM) whereas not compromising on the speed of the traditional Wallace number (TWM) has the lowest house as compared to different tree-based multipliers. A MW multiplier is degree economical hardware implementation of digital circuit multiplying two integers. generally in typical Wallace multipliers many full adders and [*fr1] adders square measure utilized in their reduction section. [*fr1] adders do not shrink the quantity of partial product bits. Therefore, minimizing the quantity of [*fr1] adders utilized in an exceedingly multiplier reduction will shrink the standard. Hence, a modification to the Wallace reduction is finished throughout that the delay is that a similar as for the quality Wallace reduction. The modified reduction methodology greatly reduces style of [*fr1] adders with a very slight increase inside the amount of full adders. Reduced quality Wallace multiplier reduction consists of three stages. first section the N x N product matrix is formed and before the passing on to the second section the merchandise matrix is

rearranged to want the shape of inverted pyramid. throughout the second section the rearranged product matrix is sorted into non-overlapping cluster of {three} as shown inside the figure three.8, single bit and a couple of bits inside the cluster square measure reaching to be passed on to subsequent stage and three bits ar given to a full adder. the quantity of rows in each stage of the reduction section is calculated by the formula

$r_{i+1}= 2[r_{i/3}]+r_i \bmod 3$

If $r_i \bmod 3=0$, then $r_{i+1}=2r_{i/3}$

If the worth calculated from the on top of equation for range of rows in every stage within the second section and therefore the range of row that ar fashioned in every stage of the second section doesn't match, solely then the [*fr1] adder are used. the ultimate product of the second stage are within the height of 2 bits and passed on to the third stage. throughout the third stage the output of the second stage is given to the carry propagation adder to get the ultimate output. Thus sixty four bit changed Wallace number is built and therefore the total range of stages within the second section is ten. As per the equation the quantity of row in every of the ten stages was calculated and therefore the use of [*fr1] adders was restricted solely to the tenth stage. the full range of [*fr1] adders employed in the second section is eight and therefore the total range of full adders that was used throughout the second section is slightly augmented than within the typical Wallace number. Since the sixty four bit changed Wallace number is troublesome to represent, a typical 10-bit by 10-bit reduction is shown in figure three.8 for understanding.

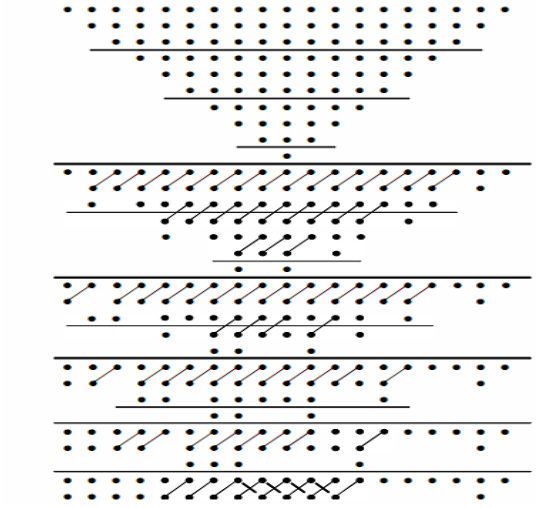


Figure 3.8 Modified Wallace Multiplier

128-Bit MAC Unit:

Here, we have a tendency to style a high performance 128 bit number and-Accumulator (MAC). we have a tendency to used 128 bit changed Wallace number. The waterproof inputs ar obtained from the memory location and given to the number block. this may be helpful in 128 bit digital signal processor. The input that is being fed from the memory location is 128 bit. once the input is given to the number it starts computing worth for the given 128 bit input and thus the output are 256 bits. The number output is given because the input to a few completely different adders that performs addition. The output of the parallel prefix adder is 257 bits.

Results:

II. CONCLUSION

In this paper implementation of sixty four bit selection and accumulate is completed victimization the new form of coat unit victimization completely utterly completely different adders considerably Kogge stone adder, goose kung adder and carry save adder. Memory usage is discovered in terms of Slices and 4 input operation tables for the all the 3 adders. BKA proves to be a stronger numerous. though the BKA's house rises as a results of the bit size increase, it doesn't rise as drastically as KSA. the upper the amount of bits supported by the PPAs, the larger is that the adder in terms of house. In terms of technique delay or time propagation delay (tpd), KSA can be associate degree improved alternative. we've an inclination to all or any perceive that alone at bit size but sixteen bits the KSA has longer tpd. so KSA is widely-known as a PPA that performs quick logical addition. Hence, victimization this new form of coat unit with the suitable selection in most of the DSP applications winds up in higher results and performance. The Performance analysis, simulation result and comparison unit reportable over. The coat unit with Kogge-stone adder has minimum delay of fifty four.58ns with raised house.

Future Work:

For the long term work the implementation of 128 bit Multiplier-and-accumulate is completed. Pipelining of 2-64bit coat unit will even be designed and additionally the following parameters is compared with the prevailing planned system. The new style of coat unit will even be designed by varied parallel prefix adders aside from express applications like low power applications and area economical architectures. The parallel prefix networks is selected in such the best approach that it will supply best lands up within the actual applications in terms of speed, area and delay parameters.

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