International Journal For Technological Research In Engineering
Volume 4, Issue 3, November-2016 *ISSN (Online): 2347 - 4718*

SRAM DESIGN APPROACH USING PULSED LATCH BASED SHIFT REGISTER

Nemani Gowtham[1], Kusuma Rambabu[2]
[2]Assistant Professor
Dept. of ECE, Srinivasa Institute of Engineering & Technology, Cheyyeru (V), Amalapuram, India

Abstract: This paper proposes an SRAM design approach using pulsed latch based shift register. The proposed SRAM is implemented using a 256-bit shift register based on pulsed latches, which reduces the area and delay consumption. The shift register uses a small number of the pulsed clock signals by grouping the latches to several sub-shift registers and using additional temporary storage latches, which solves the timing problem between pulsed latches through the use of multiple non-overlap delayed pulse clock signals instead of the conventional single pulsed clock signal.

Index Terms: SRAM, shift register, pulsed latch, clock signal, Xilinx ISE

I. INTRODUCTION

Memory structures have become an indivisible part of modern VLSI systems. Semiconductor memory is now present not just as stand-alone memory chips but also as an integral part of complex VLSI systems. While the predominant criterion for memory optimization is often to squeeze in as much memory as possible in a given area, the trend toward portable computing (without impacting performance) has led to power issues in memory coming to the forefront. The basic storage elements of semiconductor memory have remained fundamentally unchanged for quite some time. This does not imply that other forms of storage cells cannot be conceived of; rather these cells offer the best trade-off between design factors such as layout efficiency, performance, and noise sensitivity. Static random-access memory (static RAM or SRAM) is a type of semiconductor memory that uses bistable latching circuitry (flip-flop) to store each bit. SRAM exhibits data remanence, but it is still volatile in the conventional sense that data is eventually lost when the memory is not powered. The trend of Static Random Access Memory (SRAM) along with CMOS technology scaling in different processors and system-on-chip (SoC) products has fuelled the need of innovation in the area of SRAM design. SRAM bit cells are made of minimum geometry devices for high density and to keep the pace with CMOS technology scaling, as a result, they are the first to suffer from technology scaling induced side-effects. At the same time, success of next generation technology depends on the successful realization of SRAM. Therefore, different SRAM bit cell topologies and array architectures have been proposed in the recent past to meet the nano-regime challenges. SRAM is also used in personal computers, workstations, routers and peripheral equipment: CPU register files, internal CPU caches and external burst mode SRAM caches, hard disk buffers, router buffers, etc. LCD screens and printers also normally employ static RAM to hold the image displayed (or to be printed). Static RAM was used for the main memory of some early personal computers such as the ZX80, TRS-80 Model 100 and CommodoreVIC-20.

II. EXISTING SYSTEM

A shift register is the basic building block in a VLSI circuit. Shift registers are commonly used in many applications, such as digital filters, communication receivers, and image processing ICs. Recently, as the size of the image data continues to increase due to the demand for high quality image data, the word length of the shift register increases to process large image data in image processing ICs. An image-extraction and vector generation VLSI chip uses a 4K-bit shift register. A 10-bit 208 channel output LCD column driver IC uses a 2K bit shift register. A 16-megapixel CMOS image sensor uses a 45K-bit shift register. As the word length of the shifter register increases, the area and power consumption of the shift registers become important design considerations. The architecture of a shift register is quite simple. An N-bit shift register is composed of series connected N data flip-flops. The speed of the flip-flop is less important than the area and power consumption because there is no circuit between flip-flips in the shift register. The smallest flip-flop is suitable for the shift register to reduce the area and power consumption. Recently, pulsed latches have replaced flip-flops in many applications, because a pulsed latch is much smaller than a flip-flop. But the pulsed latch cannot be used in a shift register due to the timing problem between pulsed latches. The shift register solves the timing problem using multiple non-overlap delayed pulsed clock signals instead of the conventional single pulsed clock signal. The shift register uses a small number of the pulsed clock signals by grouping the latches to several sub shifter registers and using additional temporary storage latches.

A master-slave flip-flop using two latches in Fig. 1(a) can be replaced by a pulsed latch consisting of a latch and a pulsed clock signal in Fig. 1(b). All pulsed latches share the pulse generation circuit for the pulsed clock signal. As a result, the area and power consumption of the pulsed latch become almost half of those of the master-slave flip-flop. The pulsed latch is an attractive solution for small area and low power consumption. The pulsed latch cannot be used in shift registers due to the timing problem, as shown in Fig. 2. The shift register in Fig. 2(a) consists of several latches and a pulsed clock signal (CLK_pulse). The operation waveforms in Fig. 2(b) show the timing problem in the shifter register. The output signal of the first latch (Q1) changes correctly because the input signals of the first latch (IN) is constant

during the clock pulse width (TPULSE). But the second latch has an uncertain output signal (Q2) because its input signal (Q1) changes during the clock pulse width.

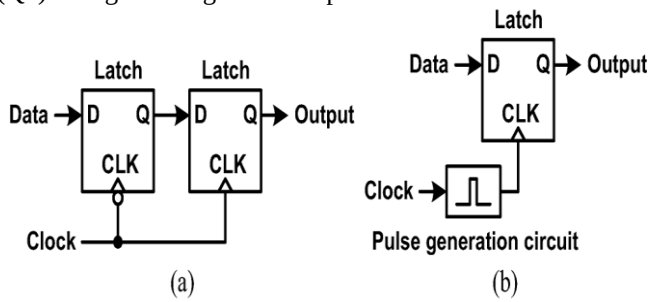

Figure1. (a) Master-slave flip-flop. (b) Pulsed latch.

One solution for the timing problem is to add delay circuits between latches, as shown in Fig. 3(a). The output signal of the latch is delayed (T_{DELAY}) and reaches the next latch after the clock pulse. As shown in Fig. 3(b) the output signals of the first and second latches (Q1 and Q2) change during the clock pulse width (T_{PULSE}), but the input signals of the second and third latches (D2 and D3) become the same as the output signals of the first and second latches (Q1 and Q2) after the clock pulse. As a result, all latches have constant input signals during the clock pulse and no timing problem occurs between the latches. However, the delay circuits cause large area and power overheads. Another solution is to use multiple non-overlap delayed pulsed clock signals, as shown in Fig. 4(a). The delayed pulsed clock signals are generated when a pulsed clock signal goes through delay circuits. Each latch uses a pulsed clock signal which is delayed from the pulsed clock signal used in its next latch. Therefore, each latch updates the data after its next latch updates the data. As a result, each latch has a constant input during its clock pulse and no timing problem occurs between latches. However, this solution also requires many delay circuits. Fig. 5(a) shows an example of shift register, which is an implementation using the pulsed latch. The shift register is divided into M sub shifter registers to reduce the number of delayed pulsed clock signals. A 4-bit sub shifter register consists of five latches and it performs shift operations with five non-overlap delayed pulsed clock signals (CLK_pulse 1:4 and CLK_pulse T). In the 4-bit sub shift register #1, four latches store 4-bit data (Q1-Q4) and the last latch stores 1-bit temporary data (T1) which will be stored in the first latch (Q5) of the 4-bit sub shift register #2. Fig. 5(b) shows the operation waveforms in the proposed shift register. Five non-overlap delayed pulsed clock signals are generated by the delayed pulsed clock generator in Fig. 6. The sequence of the pulsed clock signals is in the opposite order of the five latches. Initially, the pulsed clock signal CLK_pulse T updates the latch data T1 from Q4. And then, the pulsed clock signals CLK_pulse 1:4 update the four latch data Q4 to Q1 sequentially. The latches Q2–Q4 receive data from their previous latches Q1–Q3 but the first latch Q1 receives data from the input of the shift register (IN). The operations of the other sub shift registers are the same as that of the sub shift register #1 except that the first latch receives data from the temporary storage latch in the previous sub shift register. The shift register reduces the number of delayed pulsed clock signals significantly, but it increases the number of latches because of the additional temporary storage latches. As shown in figure 6 each pulsed clock signal is generated in a clock-pulse circuit consisting a delay circuit and an AND gate.

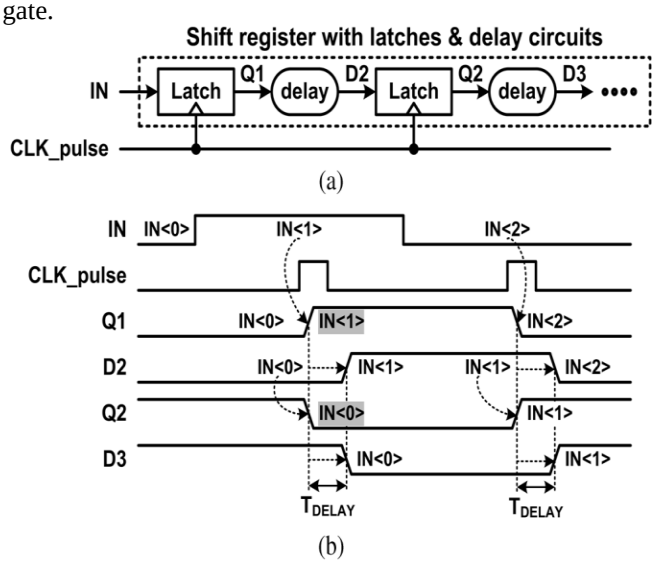

Figure2. Shift register with latches and a pulsed clock signal. (a) Schematic. (b) Waveforms.

The conventional delayed pulsed clock circuits in Fig. 4 can be used to save the AND gates in the delayed pulsed clock generator in Fig. 6. In the conventional delayed pulsed clock circuits, the clock pulse width must be larger than the summation of the rising and falling times in all inverters in the delay circuits to keep the shape of the pulsed clock. However, in the delayed pulsed clock generator in Fig. 6 the clock pulsed width can be shorter than the summation of the rising and falling times because each sharp pulsed clock signal is generated from an AND gate and two delayed signals. Therefore, the delayed pulsed clock generator is suitable for short pulsed clock signals. Figure 7 & 8 shows the simulated waveforms for 32-bit & 256-bit pulsed latch based shift register using Xilinx ISE Design suite 13.2.

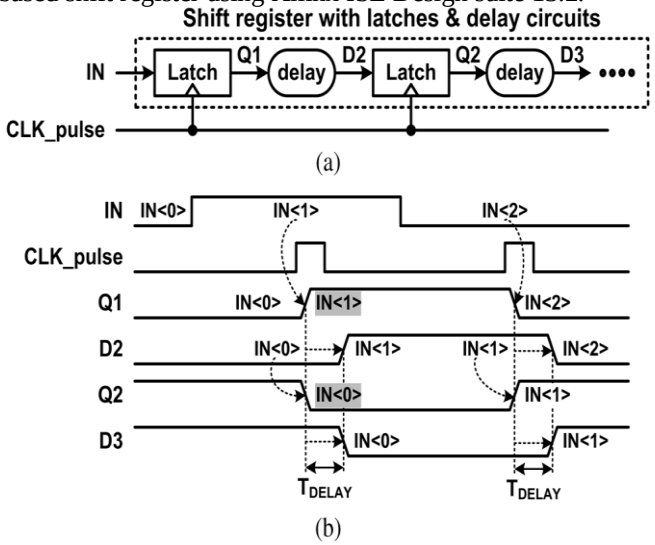

Figure3. Shift register with latches, delay circuits, and a pulsed clock signal. (a) Schematic. (b) Waveforms.

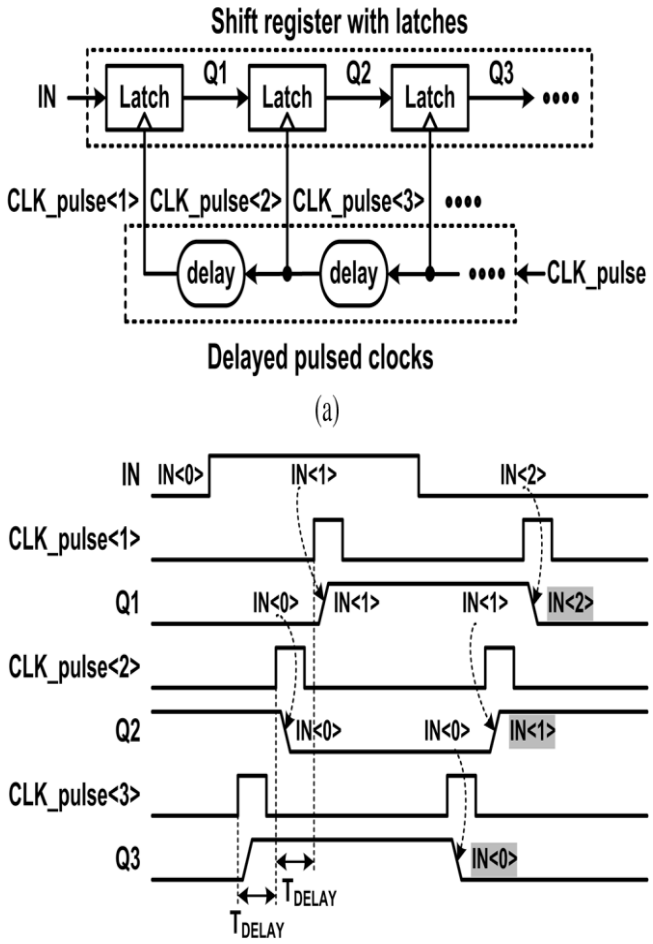

Figure4. Shift register with latches and delayed pulsed clock signals. (a) Schematic. (b) Waveforms.

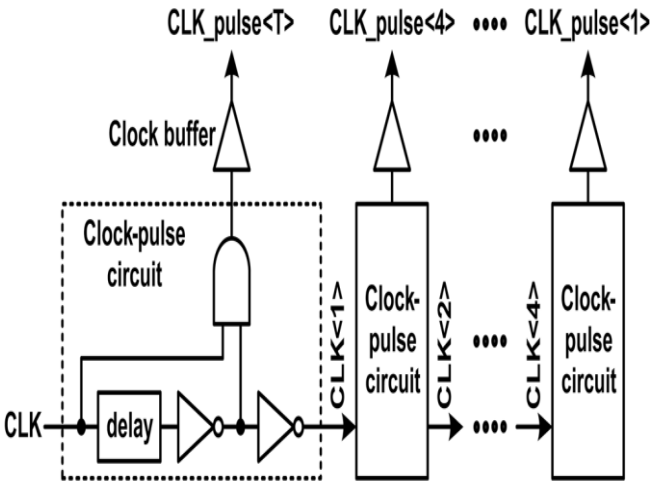

Figure 6.Delayed pulsed clock generator.

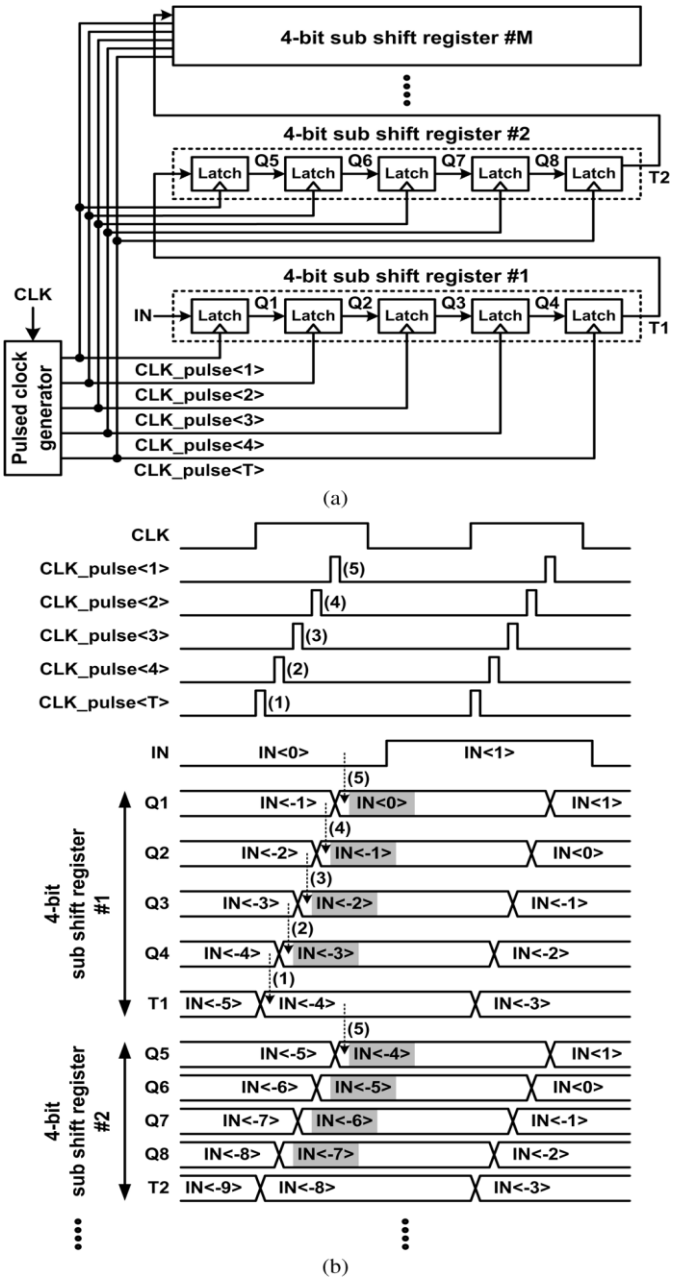

Figure 5.Pulsed latch based 256 bit shift register. (a) Schematic. (b) Waveforms.

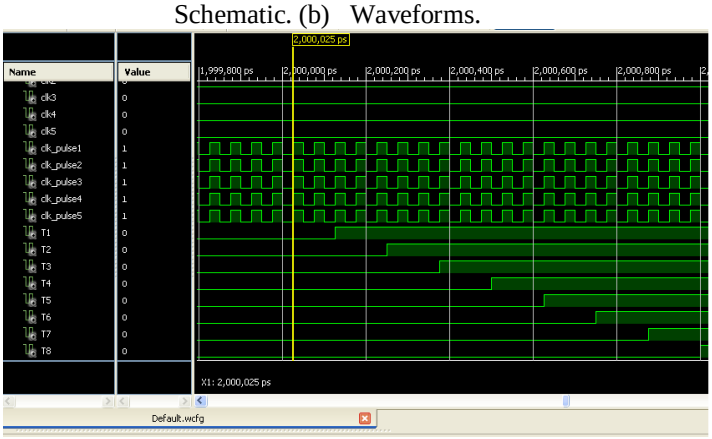

Figure 7. Simulated waveform for 256-bit shift register using Xilinx ISE Design Suite 13.2

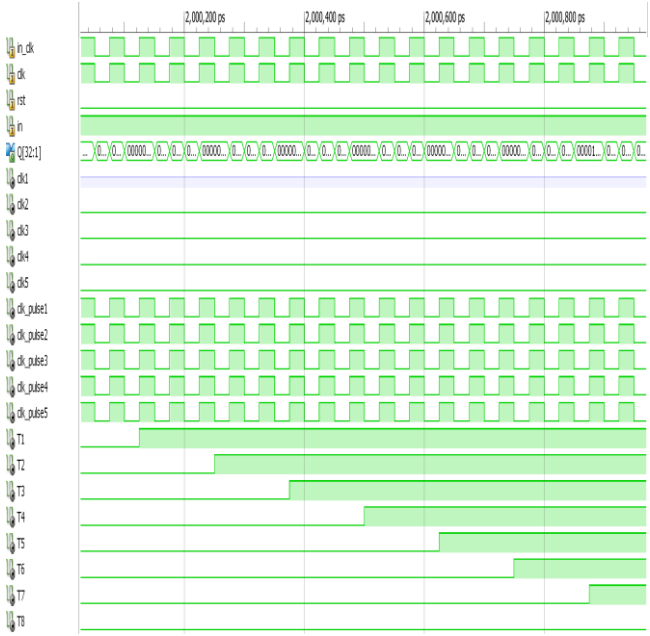

Figure8 Simulated waveform for 32-bit shift register using Xilinx ISE Design Suite 13.2

III. PROPOSED SYSTEM

The static RAM is a very important class of memory. It consists of two cross-coupled inverters, which form a positive feedback with two possible states illustrated in figure 9. This cell is also the base of many sequential circuits. The basic cell for static memory design is based on 6 transistors, with two pass gates instead of one. The proposed SRAM is implemented by grouping the pulsed latches to several sub-shift registers and using additional temporary storage latches, using Xilinx Integrated Synthesis Environment tool.

The corresponding schematic diagram is given in Figure 9 & 9(b). The circuit consists again of the 2 cross-coupled inverters, but uses two pass transistors instead of one. The cell has been designed to be duplicated in X and Y in order to create a large array of cells. Usual sizes for Megabit SRAM memories are 256 column x 256 rows or higher. The selection lines WL concerns all the cells of one row. The bit lines BL and ~BL concern all the cells of one column.

Write operation:

For writing 1/0 we should provide the data to the bit line (BL), with respect to the bit line (~BL). When the word line (WL) is enabled the data is written into respective node.

Read Operation:

When the word line (WL) is enabled, the bit line which connected to the node of the cell containing „0" is discharged. Using sense amplifiers we can know the node containing 1/0 by sensing the bit lines. The bit line containing '1' means it's connected to the node containing '1' and vice versa. The most clock frequency in the conventional shift sign up is constrained to most effective postpone of turn flops due to the fact there is no delay between flip flops. Therefore, the vicinity and electricity consumption are more critical than the velocity for choosing the turn flop. The proposed 256 bit shift register uses 4 latches and it plays shift operation with five non overlap not on time pulse clock signals (CLK_pulse). 256 latches store 256 bit statistics (Q1-Q256). The series of the pulsed clock signals is in the opposite sign of the four latches.

The shift register outputs stored to SRAM circuits finally the Shift register design get less area and less power consumption with help of pulsed clock generators. SRAM stores a bit of data on four transistors using two cross-coupled inverters. The two stable states characterize 0 and 1. During read and write operations another two access transistors are used to manage the availability to a memory cell. To store one memory bit it requires six metal-oxide-semiconductor field-effect transistors (MOFSET). MOFSET is one of the two types of SRAM chips; the other is the bipolar junction transistor.

MOFSET is a popular SRAM type. SRAM can be found in the cache memory of a computer or as part of the RAM digital to analog converter on a video card. Static RAM is also used for high-speed registers, caches and small memory banks like a frame buffer on a display adapter. Several scientific and industrial subsystems, modern appliances, automotive electronics, mobile phones, synthesizers and digital cameras also use SRAM. It is also highly recommended for use in PCs, peripheral equipment, printers, LCD screens, hard disk buffers, router buffers and buffers in CDROM / CDRW drives.

Large SRAM arrays that are widely used as cache memory in microprocessors and application specific integrated circuits can occupy a significant portion of the die area. In an attempt to optimize the performance/cost ratio of such chips designers are faced with a dilemma. Large arrays of fast SRAM help to boost the system performance. However, the area impact of incorporating large SRAM arrays into a chip directly translates into a higher chip cost. Balancing these requirements is driving the effort to minimize the footprint of SRAM cells. As a result, millions of minimum size SRAM cells are tightly packed making SRAM arrays the densest circuitry on a chip.

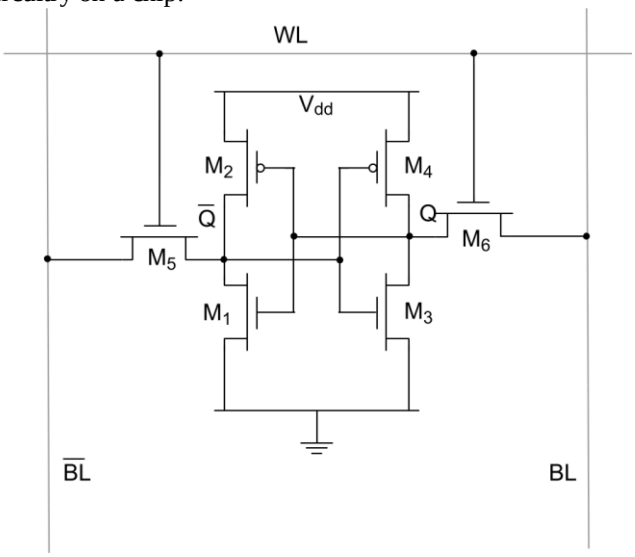

Figure 8. Layout of 6 Transistor SRAM Cell

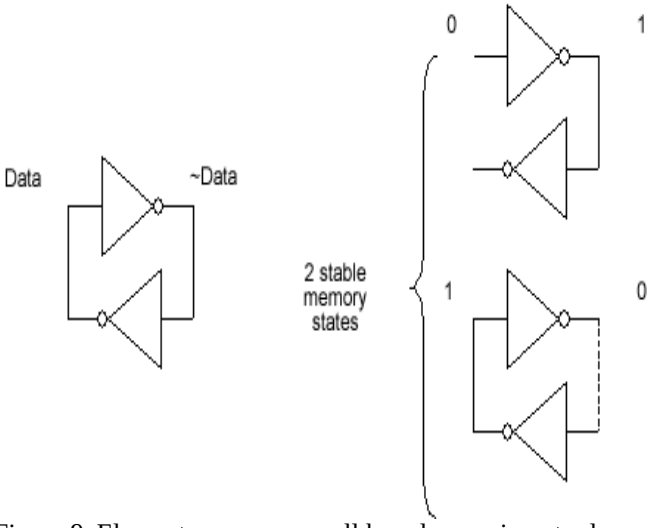

Figure 9. Elementary memory cell based on an inverter loop

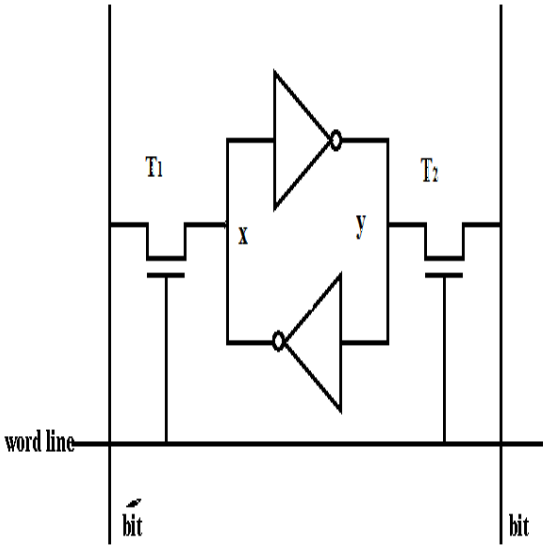

Figure 9(b). Elementary memory cell based on an inverter loop

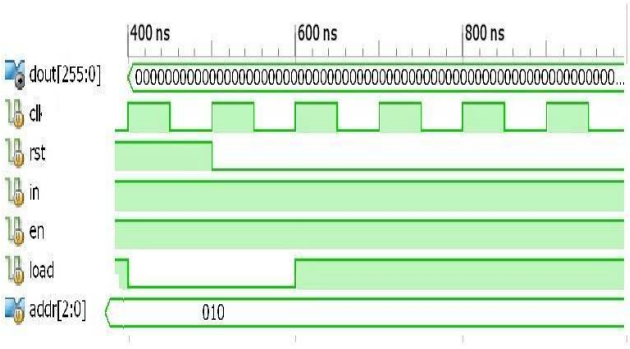

Figure10 Simulated waveform for 256 bit SRAM using Xilinx ISE Design Suite 13.2

IV. PERFORMANCE COMPARISION

The performance comparison between existing 256-bit pulsed latch based shift register & the proposed Static Random Access Memory is as follows:

Table I: Performance comparison of Existing Pulsed Latch based 256-bit shift register

Existing Pulsed Latch based 256-bit shift register		
Device Utilization Summary		
Logic Utilization	Utilized	Available
Number of 4-Input LUT's	01	9312
Number of IO's	260	
Number of bonded IOB's	258	232
Number of Slices	01	4656
Maximum Combinational path delay	6.529ns	

Table II: Performance comparison of Proposed SRAM using Pulsed Latch based 256-bit shift register

Proposed SRAM using Pulsed Latch based 256-bit shift register		
Device Utilization Summary		
Logic Utilization	Utilized	Available
Number of 4-Input LUT's	0	9312
Number of IO's	264	
Number of bonded IOB's	256	232
Number of Slices	0	4656
Maximum Combinational path delay	Nil	

The overall performance in terms of throughput can be greatly improved by providing the extra number of ports per bit cell. For the target applications such as video processing, high read access multi-port SRAM is strongly recommended since the read operation occurs more repeatedly than the write operation in video codec. For instance, in video codec once video frames are written in memory, several search algorithms have to read the data many times for decoding those frames.

V. CONCLUSION

This paper proposed an SRAM design approach using pulsed latch based 256-bit shift register. The shift register reduces the usage of number of components so that the area consumption can be reduced by replacing flip-flops with pulsed latches. The timing problem between pulsed latches is solved using multiple non- overlap delayed pulsed clock signals instead of a single pulsed clock signal. A small number of the pulsed clock signals are used by grouping the latches to several sub shifter registers and using additional temporary storage latches. A 256-bit SRAM is implemented using pulsed latch based shift register using Xilinx ISE Design Suite.

ACKNOWLEDGMENT

I thank the management, the Principal and staff of Srinivasa Institute of Engineering and Technology, Cheyyeru (V), Amalapuram, India for encouraging me for this research work. I express my sincere vote of thanks to Mr. K.Rambabu, for his kind support and encouragement in carrying out this research work.

REFERENCES

[1] Byung –Do Yang, "Low-Power and Area Efficient Shift Register Using Pulsed Latches", IEEE Trans. on circuits and systems—I: regular papers, vol. 62, no. 6, June 2015.
[2] "Low Voltage, Low Power VLSI Subsystems", Kiat-Seng Yeo, Kaushik Roy
[3] "Low Power CMOS VLSI Circuit design", Kaushik Roy, Sharat C. Prasad
[4] "A Verilog HDL Primer"-J. Bhasker
[5] "CMOS VLSI design"-Neil H.E.Weste, David Harris, Ayan Banerjee
[6] "Contemporary logic design"- R.H.Katz, Addison-Wesley publishing Co., 1993
[7] "High level synthesis: Introduction to chip & system design"- D.D. Gajski, N.D.Dutt, A.c.Wu & A.Y.Yin, Kluwer academic publishers, 1992
[8] Stojanovic and V. Oklobdzija, "Comparative analysis of master slave latches and flip-flops for high-performance and low-power systems," IEEE J. Solid-State Circuits, vol. 34, no. 4, pp. 536–548, Apr.1999.
[9] Y. W. Kim, J. S. Kim, J. W. Kim, and B.-S. Kong, "CMOS differential logic family with conditional operation for low-power application," IEEE Transactions on Circuits and Systems II: Express Briefs, vol. 55, No. 5, 2008, pp. 437-441
[10] P. Girard, "Low power testing of VLSI circuits: Problems and solutions," in First International Symposium on Quality Electronic Design, March, 2000, pp. 173-179.
[11] Sung-Mo Kang, Yusuf Leblebici (2005), CMOS Integrated Circuits-Analysis and design, Tata McGraw-hill Edition, 3rd Edition.
[12] Andrei Pavlov, Manoj Sachdev (2008), CMOS SRAM Circuit Design and parametric test in nano Scaled technologies-Process-aware SRAM design and test, Springer publications
[13] Jawar Singh, Saraju.P.Mohanty, Dhiraj K.Pradhan, "Robust SRAM designs and analysis"
[14] Andrei Pavlov, Manoj Sachdev, "CMOS SRAM Circuit Design and Parametric Test in Nano-Scaled Technologies"

