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DESIGN OF EFFICIENT NOVEL BINARY ADDERSIN QUANTUM-DOT CELLULAR AUTOMATA

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Abstract: Nowadays exponential advancement in QCA computation has led to higher fabrication and integration method. Quantum-dot cellular automaton (QCA) is an up-coming nanotechnology in the area of Nano electronics and is found to be an alternative solution to replace conventional CMOS technology for several reasons. It has attractive features such as faster speed, smaller size, and low power consumption compared to transistor-based technology. The experiments carried out in QCA demonstrated and realized the fundamental digital blocks. This paper demonstrates designing combinational circuits based on quantum-dot cellular automata (QCA), which covers a way to implement logic and all interconnections with homogeneous layer of cells.This paper presents 6-bit, 16-bit, 32-bit, 64-bit adders using M-cell(majority gate). The comparative study shows that the adder in QCA exhibits superior performance considering all the potency parameters of Ripple carry adder.

Keywords: Quantum Computing, binaryadders, Low Power, majority gates.

I. INTRODUCTION

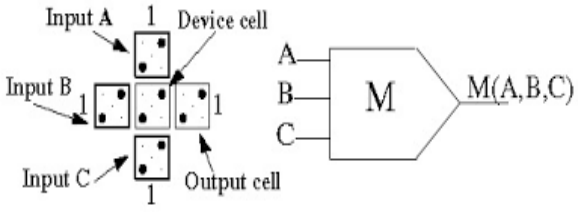
In recent time each style of computation is obtaining advanced and researchers face monumental challenges over billions of arithmetic operationsper second. According toGordon Moore, the junction transistor count and performance of logic circuits is doubled in each 2 years, this method can continue till semiconductor circuits reach to its physical limit. Quantum–dot Cellular Automata (QCA) is a novel nanotechnology that has attracted a lot of attention over the last two decades. This technology promises extremely low power consumption, high speed and extremely dense structure for implementing any logical circuit. Current CMOS devices are becoming resistant to scaling. The most important reason is the power density. Nanotechnology is a possible alternative to these problems and the(International road map for semiconductors) ITRS report summarizes several potential solutions. QCA is an interesting option and was introduced in 1993. QCA creates general computational functionality at the Nano scale by simply controlling the position of single electron. Circuits based on the QCA technology solve series of problems which the traditional devices face when it enters the domain of Nano meter scale. QCA has gained significant popularity in recent years, which is due to the growing interest in creating computing devices and implementing any logical function in QCA. The basic structure of the QCA cell is a set of four charge containers called quantum dots positioned at the corners of a square. Arrays of QCA cells can be introduced to perform all Boolean functions. This results in Columbic interactions, which influences the polarization of neighboring cells. QCA designs have been proposed with potential barriers between the dots that can be controlled and used to clock QCA designs. QCA cells are used for both logic designs and interconnections that can exploit either the coplanar cross or bridge technique. The fundamental logic gates inherently available with in the QCA technology are the NOT gate and the MG.

II. CELLULAR AUTOMATA

The information storage and transport on quantum-dot cellular automata isn't supported the flow of electrical particle current, however on the native position of the charged particles within alittle section of the circuit, referred to as a cellular automaton. This QCA cell includes a restricted variety of quantum-dots, that the particles will occupy, and these dots are organized such the cell will have solely 2 polarizations (two degenerate quantum mechanical ground states), representing binary worth zero or one. A cell will switch between the 2 states by belongings the charged particles tunnel between the dots quantum automatically.

The cells exchange information by classical Columbic interaction. associate degree input cell forced to a polarization drives subsequent cell into an equivalent polarization, since this mixture of states has minimum energy within the field between the charged particles in neighboring cells. Information is derived and propagated in a very wire consisting of the cell automata. The accessible 2 cell sorts, that square measure orthogonal and have stripped interaction with one another, facultative the planar wire crossing, wherever the wires incorporates totally different cell sorts and may operate severally on an equivalent fabrication layer. a conventional multi-layer crossing will be created with either cell sort, however the technology has not been incontestable.

Majority Gate



The basic component of a nanostructure supported QCA may be a sq. cell with four quantum dots and 2 free electrons. The latter will tunnel through the dots among the cell, but, as a result of Columbic repulsion, they're going to forever reside

in opposite corners, so resultingin stable states, conjointly named polarizations. Locations of the electrons within the cell are related to the binary states one and zero.

Adjacent cells move through static forces and have a tendency to align their polarizations. However, QCA cells don't have intrinsic information flow directivity. Therefore, to attain manageable information directions, the cells among a QCA style square measure partitioned off into the questionable clock zones that square measure more and more related to four clock signals, every part shifted by 90◦ . This clock theme, named the zone continuance theme, makes the QCA styles per se pipelined, since every clock zone behaves sort of a D-latch.

QCA cells area unit used for each logic structures and interconnections that may exploit either the planar cross or the bridge technique. the basic logic gates inherently offered inside the QCA technology area unit the electrical converter and also the majority gate (MG). Given 3 inputsa, bandc, the MG performs the logic operate reported in as long as all input cells area unit related to identical clock signal clkx (with x starting from zero to 3), whereas the remaining cells of the MG area unit related to the clock signal clkx+1.

M(a,b,c) = a . b + a . c + b .c

QCA Logic Devices: The fundamental QCA logic primitives include a QCA wire, QCA inverter and QCA majority gate (Cho and Swartzlander, 2007; Walus et al., 2004b; Reza and Vafaei 2008), as described below.

QCAWire: In aQCA wire, the binary signal propagates from input to output because of the electrostatic interactions between cells. The propagation in a 90° QCA wire is shown in Fig. 2. Other than the 90° QCA wire, a 45° QCA wire can also be used. In this case, the propagation of the binary signal alternates between the two polarizations.

QCA Inverter: The QCA cells can be used to form the primitive logic gates. The simplest structure is the inverter, which is usually formed by placing the cells with only their corners touching. The electrostatic interaction is inverted, because the quantum-dots corresponding to different polarizations are misaligned between the cells.

QCA majority gate: The QCA majority gate performs a three-input logic function. Assuming the inputs is A, B and C, the logic function of the majority gate is: M (A, B, C) = AB+BC+CA (1) The tendency of the majority device cell to move to a ground state ensures that it takes on the polarization of the majority of its neighbors. The device cell will tend to follow the majority polarization because it represents the lowest energy state. By fixing the polarization of one input to the QCA majority gate as logic "1" or logic "0," an AND gate or OR gate will be obtained, respectively, as follows: M(A,B,0) = AB (2a) M(A,B,1) = A+B (2b).

Thus, we can base all QCA logic circuits on threeinput majority gates. In order to achieve efficient QCA design, majority gate-based design techniques are required. The study of majority gates mainly focuses on the threshold logic

Majority gate design: Digital computers perform various arithmetic operations. The most basic operation is the addition . The addition operation is achieved by majority logic that can reduce the overall number of gates required to create the adder.

Half-adder: The half adder is a combinational circuit that performs addition of two bits. It is designed conventionally by EXOR and AND gates. When two inputs A and B are added, the Sum and Carry outputs are produced according to the truth table. The logic function for half-Adder is: Sum = A'B+AB' Carry = AB The majority gate expression for above equation is: Sum = M (M (A, B', 0), M (A', B, 0), 1) Carry = M ((A, B, 0)

Full-adder: The full adder circuit is implemented by digital logic gates. When three inputs A, B and C are added, the Sum and Carry outputs are produced according to the truth table. We have designed the full adder based on QCA addition Algorithm given in below

III. QCA ADDITION ALGORITHM

Majority logic of carry:

Cout= AB+BC+AC)
= M (M (B, M(A,C,1) ,0) , M(A,C,0) , 1)
= M(A,B,C)

Majority logic of sum:

Sum= ABC+A'B'C+A'BC'+AB'C'

Direct implementation:

Sum = M(M(A,M(M(B,C,0), M(B',C',0) ,1, 0)

Majority gates: M (A' M (M (B',C,0),1) ,0),1)

Reduction Technique:

Sum = ABCin+A'B'Cin+A'BC'in+AB'C'in
= (A.B + A'.B') Cin + (A'.B + A.B') C'in
= [A.B + A '.B ' + A.C ' in + A '.C ' in
+ B.C ' in + B ' C ' in] Cin + (A '.B +
A.B ')C ' in]
= [(A '.B ' + A '.C ' in + B '.C ' in) + (A.B
+ A C ' in + B C ' in)] Cin + (A '.B
+ A.B ')C ' in]
= [(A '.B ' + A '.C ' in + B '.C ' in) + (A.B
+ A C ' in + B C ' in)] Cin + (A.C 'in
+ B.C 'in) +(A '.Cin + B '.C 'in)]
= [(A '.B ' + A '.C ' in + B '.C ' in) Cin
+ (A.B + A C ' in + B C ' in)] Cin + (AB
+ A.C 'in + B.C 'in) (A '.C 'in + B '.C 'in
+ A 'B ')]
=M (A, ' B ',C 'in) .Cin + M(A,B,C ' in).
Cin + M(A ',B ',C ' in) M(A,B,C ' in)]
= M [M (A ',B ',C ' in), Cin, M(A,B,C '
in)]

Sum =M [C ' out, Cin, M (A, B, C ' in)] 3 majority gates

This reduction technique is used to reduce the number of majority gates from 11-3. QCA implementation of adders: Here we apply The Majority logic method for constructing QCA adders. The proposed adders are implemented with QCA cells and number of cells has reduced by cell minimization techniques.

IV. SIMULATION RESULTS

The planned styles of QCA adders are functionally verified through simulations in vcs. The simulation results show that the comparators offer good output for all attainable mixtures of inputs. The simulation results for 6-bit, 16-bit, 32-bit and 64-bit adder shown below

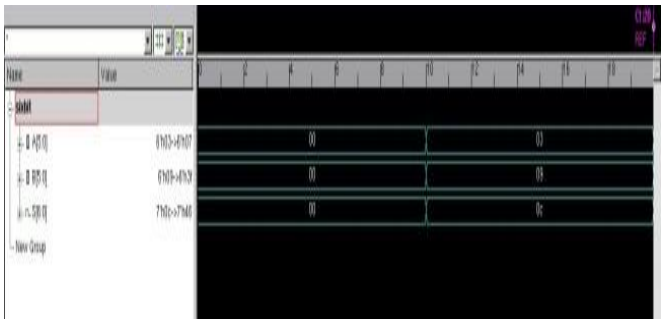


Fig.1 Simulation Result of 6-bit QCA Adder

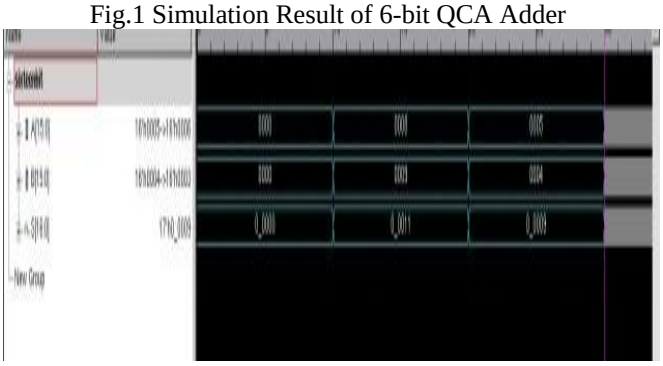


Fig.2 Simulation Result of 16-bit QCA Adder

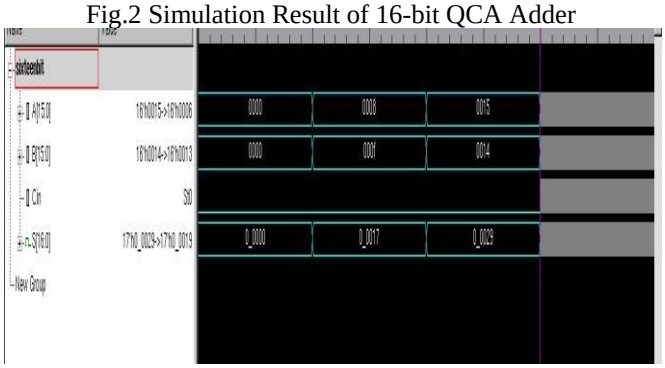


Fig.3 Simulation Result of 16-bit normal Adder

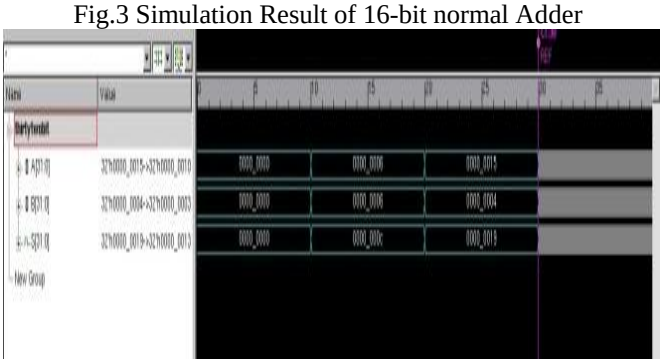


Fig.4Simulation Result of 32-bit QCA Adder

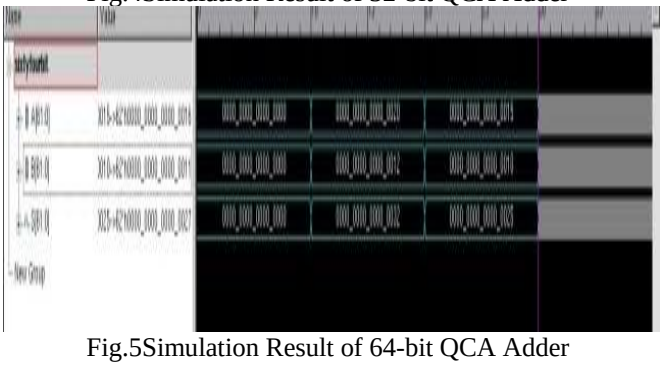


Fig.5Simulation Result of 64-bit QCA Adder

V. SCHEMATIC REPORTS

The planned styles of QCA adders are synthesized in dc compiler and schematic results are shown in below figures respectively, And comparition results are shown in tabular form varying area, arrival time, dynamic power of 6bit, 16bit, 32bit ,64bit adders with 16bit normal adder and 16bit adder using QCA

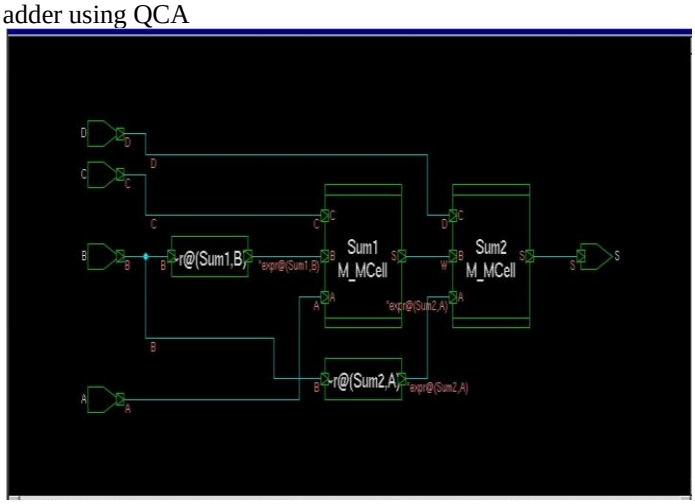


Fig.6 Schematic Report of sum Mcell using QCA

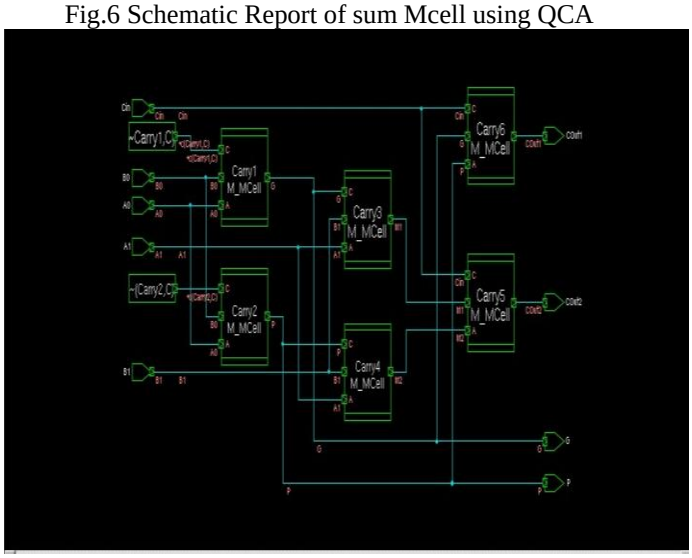


Fig.7 Schematic Report of carry Mcell using QCA

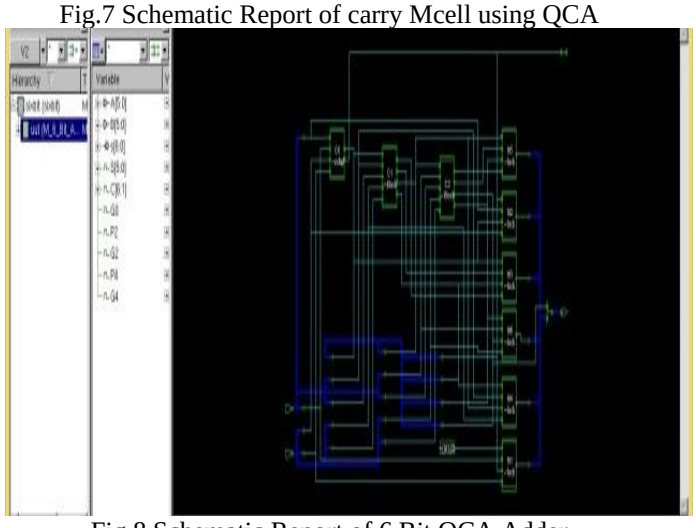


Fig.8 Schematic Report of 6 Bit QCA Adder

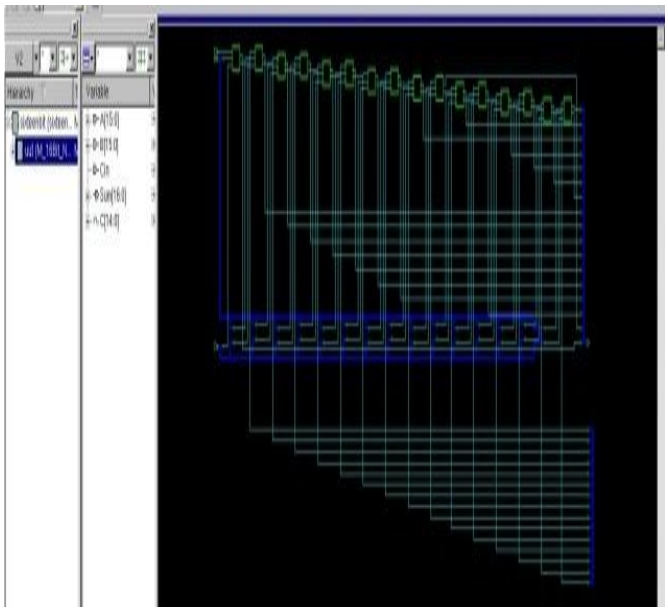


Fig.9 Schematic Report of 16-bit QCA Adder

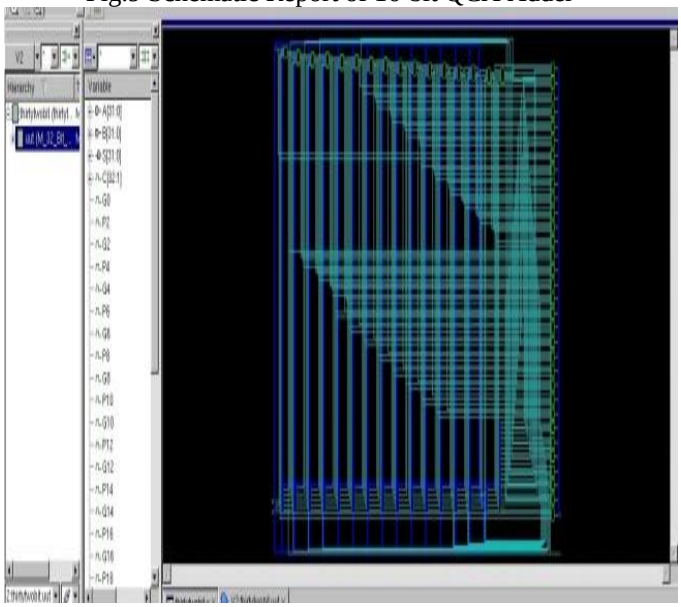


Fig.10 Schematic Report of 32-bit QCA Adder

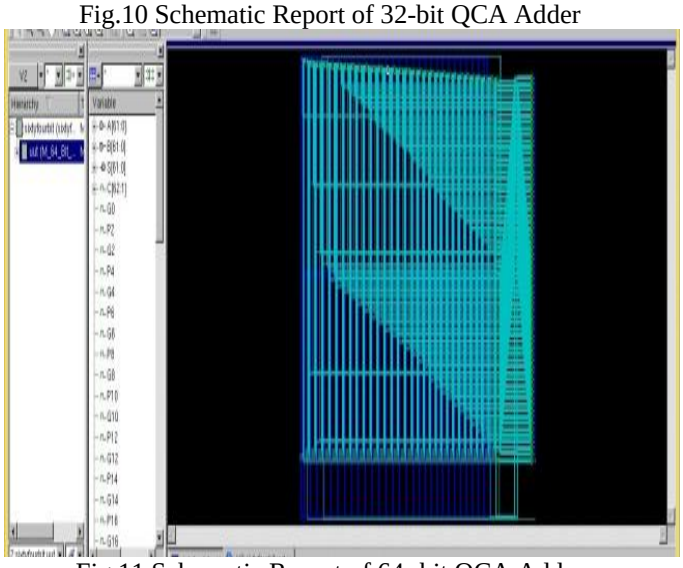


Fig.11 Schematic Report of 64 -bit QCA Adder

VI. SYNTHESIS REPORTS

Comparison of QCA based adders

Results	6-bit QCA	32-bit QCA	64-bit QCA
Total area	559.9522	3338.3242	6538.8007
Data arrival time	7.34 sec	21.56 sec	38.04 sec
Total Dynamic Power	30.821uW	197.10 uW	391.60 uW

Comparison of 16 bit normal adder and 16 bit QCA adder

Results	16-bit Normal Adder	16-bit QCA Adder
Total area	900.3468	654.6552
Data arrival time	12.76 sec	9.02 sec
Total Dynamic Power	94.8359 uW	68.7087 uW

VII. CONCLUSION

This paper presents a systematic approach of different arithmetic adders have been designed using majority gates. The functionality checks were done using Synopsys tool and the designs are compared according to the complexity, area and number of clock cycles. The operations of these circuits have been verified according to the truth table. The performance analyses of those circuits are compared .The proposed schematics are significantly smaller than the circuits using CMOS technology and it reduces the area as well as complexity required for the circuit than the previous QCA circuits.

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