International Journal For Technological Research In Engineering
Volume 4, Issue 4, December-2016 *ISSN (Online): 2347 - 4718*

AN OPTIMIZED UNIVERSAL SHIFT REGISTERS USING PULSED LATCHES

G.Vishnu Chakra Rao[1], P.Pushpalatha[2]
[1]PG Scholar, [2]Assistant Professor, Dept. of ECE, JNTUK, Kakinada, AP, India

Abstract: ***This paper proposes a low-power and more proficient shift register utilizing advanced digital pulsed latches. The area and power utilization are decreased by replacing flip-flops with pulsed latches. This scheme takes care of the timing issue between pulsed latches using numerous non-overlap delayed pulsed clock signals rather than the traditional single pulsed clock signal. The shift register utilizes a small number of the pulsed clock signals by gathering the latches to few sub shifter registers and utilizing extra short-term storage latches.A 256-bit universal shift register utilizing pulsed latches was designed. The power utilization is 80µW at a 28 MHz clock frequency. In advanced circuits, a shift register is a course of flip-flops, sharing a similar clock, in which the input of every flip-flop is associated with the "data" contribution of the following flip-flop in the chain, In a circuit that shifts by one position the "bit array" stored in it, moving in the bit at its input and moving out the last bit in the array, at every move of the clock input. More generally, a shift register might be multidimensional, so that it's "data in" and stage outputs are themselves bit arrays this is actualized essentially by running a few shift registers of a similar bit length in parallel.***

Keywords: Area-efficient, flip-flop, pulsed clock, pulsed latch, shift register.

I. INTRODUCTION

Flip-flops are the fundamental data saving components utilized broadly as a part of a wide range of digital designs. According to Moore's Law the feature size of CMOS technology process decreased, Implementers can incorporate several transistors onto the same die. The more transistors results more toggling and more power dispersed as heat or radiation. Heat is one of the phenomenon bundling challenges in this age, it is one of the fundamental difficulties of low power design techniques and practices. Another driver of low power research is the dependability of the integrated circuit. Additional toggling infers higher average current is removed and along these lines the probability of dependable issues arises. We are moving from computers to tablets and also smaller digital computing systems. With this significant pattern proceeding and without a match drifting in battery life, all the low power issues should be tended to. The present patterns will be in the long run command low power design mechanism on a substantial scale to coordinate the patterns of power utilization of today's and future integrated chips. Power utilization of Very Large Scale Integrated plan is given by General connection, $P = CV^2f$ [1]. Since power is corresponding to the square of the voltage according to the relation, voltage scaling is the most noticeable approach to decrease power dispersal. However, voltage scaling results in threshold voltage scaling which bows to the exponential increment in leakage power. In spite of the fact that few contributions have been made to the art of single edge triggered flip-flops, a need apparently happens for an outline that further enhances the execution of single edge triggered flip-flops designs. The architecture of a shift registers is very simple. An N-bit shift registers is made out of series connected N data flip-flops. The speed of the flip-flop is less essential than the area and power utilization because there is no circuit between flip-flips [6] in the shift registers. The smallest flip-flop [7] is appropriate for the shift register to decrease the area and power utilization. Recently, shift register have replaced flip-flops [9] in numerous applications, because pulsed latch is much smaller than a flip-flop. In any case, the pulsed latch can't be utilized as a part of a shift register because of the timing issue between pulsed latches.

II. SHIFT REGISTERS

A shift register is the fundamental building block in a VLSI circuit. Shift registers are normally utilized as a part of several applications, such as communication receivers [2], image processing [3], and digital filters ICs [1] Recently, as the size of the picture information keeps on expanding because the high demand for high quality image data, the word length of the shift register increments to process substantial image information in image preparing ICs. An image extraction and vector reproduction VLSI chip utilizes a 4K-bit shift register [4]. A 10-bit 208 channel output LCD section driver IC utilizes a 2K-bit shift register a 16-megapixel CMOS image sensor utilizes a 45K-bit shift register [5].

As the word length of the shift register expands, the power and area utilization of the shift register become important design considerations. The smallest flip-flop is appropriate for the shift register to diminish the power and area Utilization.

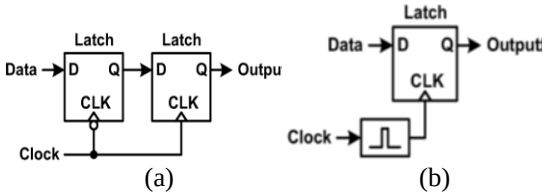


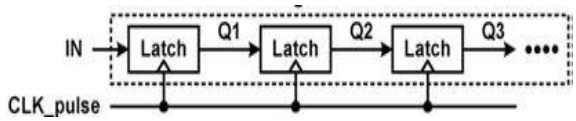
Fig 1. (a) Master-slave flip-flop. (b) Pulsed latch.

Shift registers can have both parallel and serial inputs and outputs. These are frequently arranged as parallel-in, serial-out' (PISO) or as 'serial-in, parallel-out' (SIPO).There are also types that have both parallel and serial inputs and types with serial and parallel output. There are also "bidirectional"

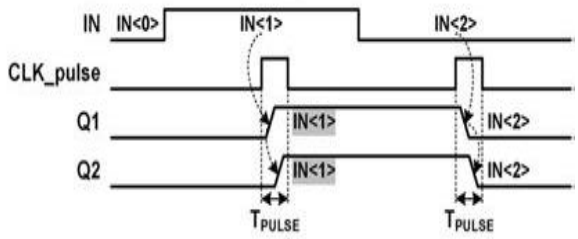
shift registers which allow shifting in both directions: L→R or R→L. The serial input and last output of a shift register can also be connected to create a 'circular shift register' previous work regularly measured energy utilization using a restricted arrangement of information examples with the clock toggling each cycle. But real designs have a wide variation in clock and data action across various TE instances. Sequential logic, not at all like combinational logic is influenced by the present inputs, as well as, by the earlier history. As such, sequential logic recalls past events. Pulsed latch structures employ an edge-triggered pulse Generator to give a short transparency window. Contrasted with master–slave flip-flops, pulsed latches have the advantages of requiring just a single latch stage for every clock cycle and of allowing time-borrowing across cycle boundaries. The real disadvantages of pulsed latches are the increased susceptibility to timing hazards and the energy dissipation of the local clock pulse generators.

III. PROPOSED ARCHITECTURE

A master-slave flip-flop utilizing two latches as a part of Fig.1 (a) can be replaced by a pulsed latch consisting of a pulsed clock signal and latch in Fig. 1(b) [6]. All pulsed latches share the pulse generation circuit for the digital pulsed clock signal. Thus, the power and area utilization of the pulsed latch turn out to be half of those of the master-slave flip-flop. The pulsed latch is a best solution for low power and small area consumption. The pulsed latch can't be utilized as a part of shift registers because of the timing violations, as appeared in Fig. 2. The shift register in Fig. 2(a) contains of pulsed clock signals and many latches (CLK pulse). The operation waveforms in Fig. 2(b) demonstrate the timing violations in the shift registers. The first latch output signal (Q1) changes accurately because the first latch input signal (IN) is consistent during clock pulse width (TPULSE). But, the second latch has an uncertain output signal (Q2) because (Q1) its input signal changes during the clock beat width.



2(a)

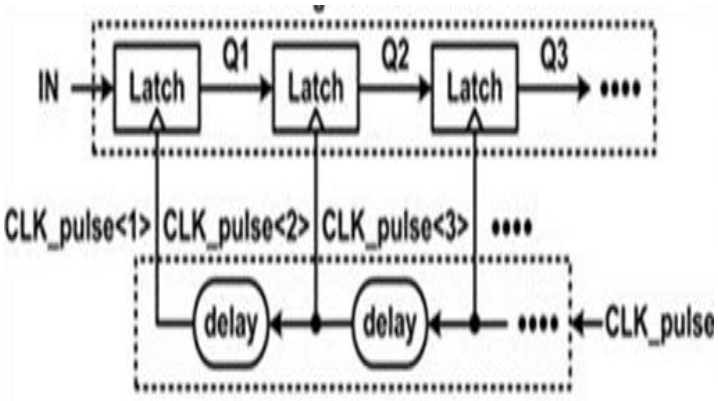


2(b)

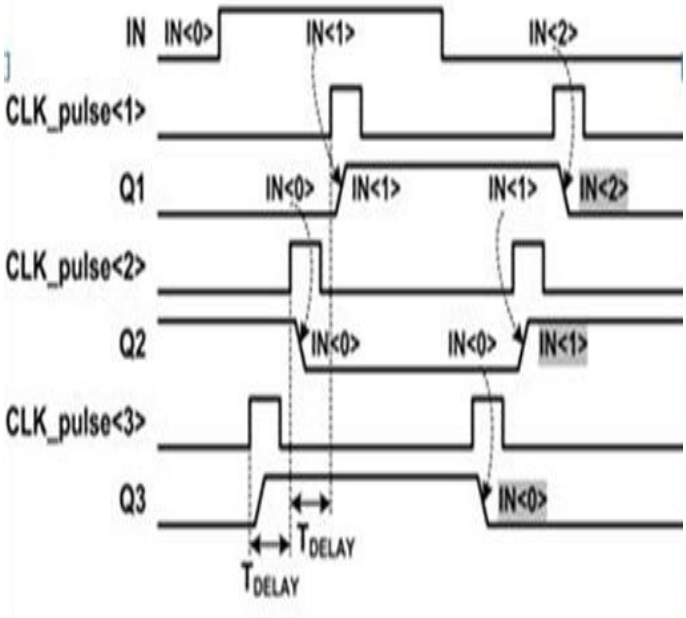
Fig. 2. Shift register with latches and a pulsed clockSignal. (a) Schematic. (b)Waveforms

One solution for the timing issue is to include delay circuits between latches, as appeared in Fig. 3(a). The output signal of the latch is delayed and reaches the following latch after the clock pulse. As appeared in Fig. 3(b) the output signals of the second and first latches (Q2 and Q1) change during the clock pulse width, but the input signal of the third and second latches (D3 and D2) because the same as the output signal of the second and first latches (Q2 and Q1) after the clock pulse as a results, all latches have constant input signals during the clock pulse and no timing issue happens between the latches. However, the delay circuits cause power over heads and large area.

A 4-bit universal sub shift consists of five latches and it performs move operations with five non overlap delayed digital pulsed clock signals (CLK_pulse<1:4>and CLK_pulse<T>). In the 4-bit sub shift register #1, four latches store 4-bit information (Q1-Q4) and the last latch stores 1-bit temporary input (T1) which will stored in the first latch (Q5) of the 4-bit sub shift register #2. Fig. 4(b) demonstrates the operation waveforms in the proposed shift register.



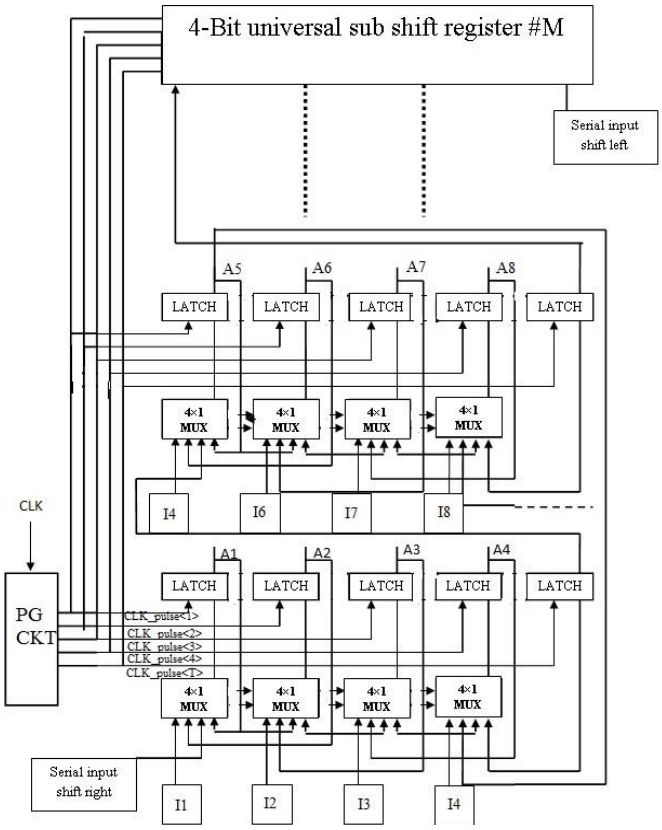
3(a)



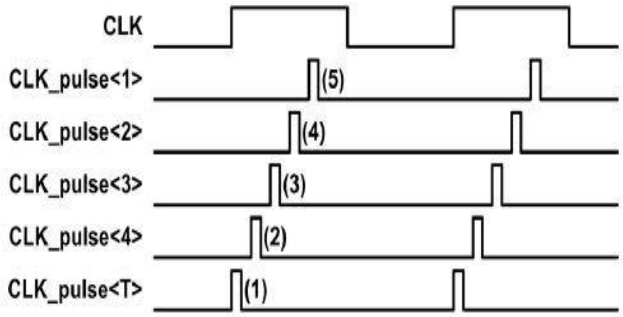
3(b)

Fig. 3. Shift register with latches, delay circuits, and a pulsed clock signal. (a)Schematic. (b)Waveforms

The quantities of latches and clock-pulse circuit's change as indicated by the word length of the sub shift register is selected by considering the power consumption, speed, area.



4(a)



4(b)

Fig. 4(a).256-universal shift register using pulsed lateches
4(b).waveforms

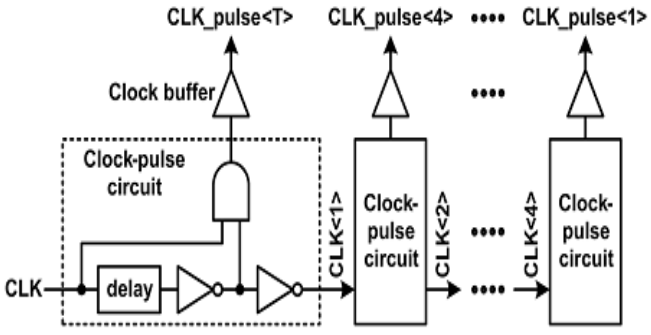


Fig.5. Delayed pulsed clock generator

Area optimization: The area enhancement can be executed as takes after. At the point when the circuit areas are standardized with a clock, the area of latch and a clock-pulsed circuit are 1 and 2 individually. The total area becomes $(\alpha_A \times (K+1) + N(1+\frac{1}{k})$. The optimal K $(=\sqrt{N/\alpha_A})$ for the minimum area is acquired from the first order differential equation of the $(0=\alpha_A - N/K)$.an integer for the minimum area is selected as a divisor, which is nearest to$\sqrt{N/\alpha_A}$.

Power optimization: The power optimization is Similar to the area optimization. The power is consumed mostly in clock-pulse circuits and latches. Every latch consumes power for clock loading and data transmission. When the circuit power are balanced with latch, the power consumption of a clock-pulse and a latch respectively. The total power consumption is also $(\alpha_P \times (K+1) + N(1+\frac{1}{k})$.Aninteger for the minimum power is selected as a divisor of, which is nearest to$\sqrt{N/\alpha_P}$.

Chip Implementation: The maximum clock frequency in the conventional shift register is limited to only the delay of flip-flops because there is no delay between flip-flips. Therefore, the power and area consumption are more important than the speed for selecting the flip-flop. The proposed shift register uses latches instead of flip-flops to reduce the power and area consumption.

VCS Simulation Results

Top Module:

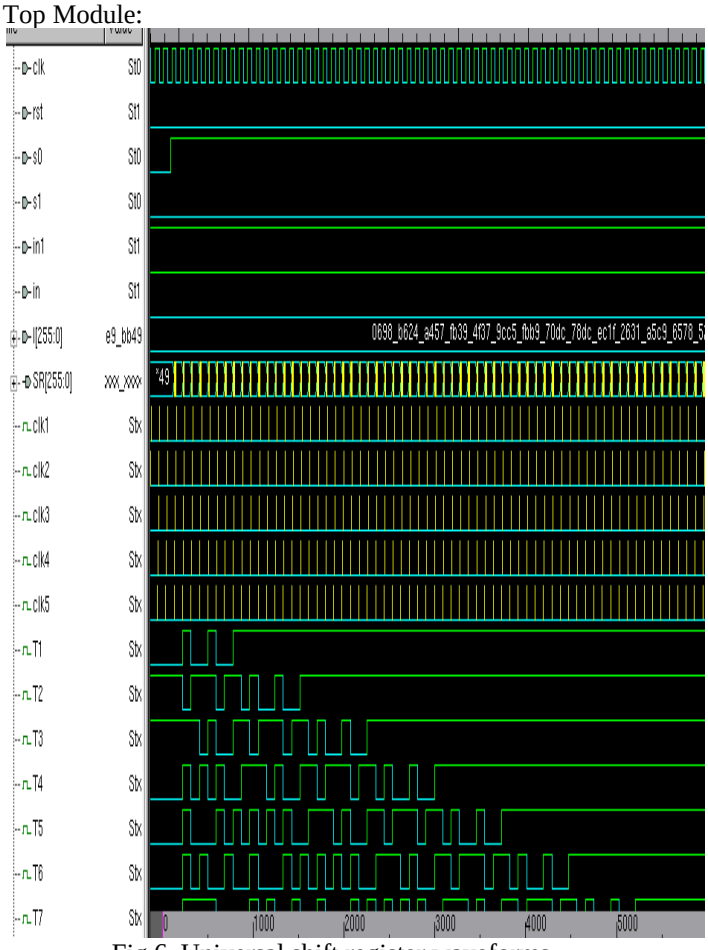


Fig 6. Universal shift register waveforms

RTL Schematic:

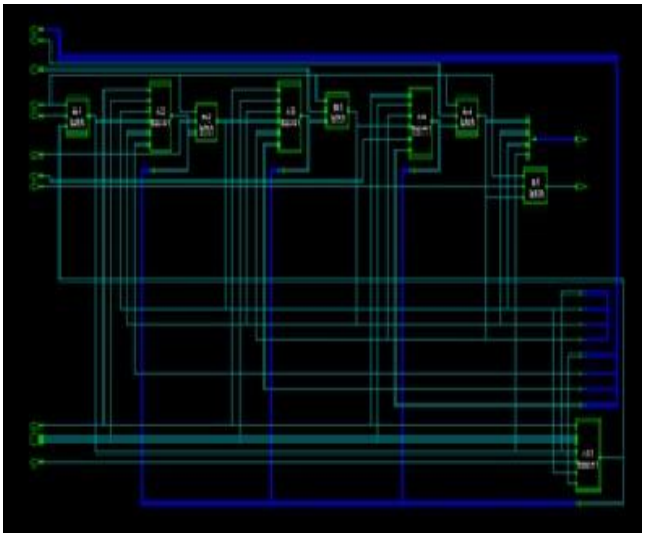


Fig 7. Universal 4 bit sub shift register schematic

Design Summary:

TABLE 1: PERFORMANCE COMPARISONS OF UNIVERSAL SHIFT REGISTER

	Conventional shifter register	Proposed universal shifter register	
	Flip-flops	Pulsed latches	
Word length of the shift register	256		
Word length of the sub shift register	-	4-bit	8-bit
Total number of pulsed latches	256	320	288
Area(μm^2)	26563	19908	18293
Power(µW)	82.74	75.18	67.57
Timing(ns)	34.71	17.19	15.34

IV. CONCLUSION

This paper proposed a universal shift register using digital pulsed latches. The shift register reduces power and area consumption by replacing flip-flops with pulsed latches .The timing problem between pulsed latches is solved using several non-overlap delayed pulsed clock signals as an alternative of a single pulsed clock signal.

REFERENCES

[1]. Xiaowen Wang, and William H. Robinson, "A Low-Power Double Edge Triggered Flip-Flop with Transmission Gates and Clock Gating" IEEE Conference,pp 205-208, 2010.

[2]. PhaedonAvouris, JoergAppenzeller, Richard Martel, and Shalom J. Wind. "Carbon nano-tube electronics". Proceedings of the IEEE, 91(11):1772–84, November 2003.

[3]. Fabien Pregaldinyet.al., "Design Oriented Compact Modelsfor CNTFETs", IEEE Trans. Elec. dev. 2006.

[4]. Flop Based on Signal Feed-Through Scheme "International Journal of Advanced Research in Electronics and Communication Engineering (IJARECE) Volume 3, Issue 11,November 2014.

[5]. ManojkumarNimbalkar, VeereshPujari"Design of lowpower shift register using implicit and explicit type flip flop",Vol 05, Article 05357June 2014

[6]. S. Heo, R. Krashinsky, and K. Asanovic, "Activity-sensitive flip-flop and latch selection for reduced energy," IEEE Trans.Very Large Scale Integr. (VLSI) Syst., vol. 15, no. 9, pp. 1060–1064, Sep. 2007.

[7]. S. Naffziger and G. Hammond, "The implementation of thenextgeneration 64 b itanium microprocessor," in IEEE Int.Solid-State CircuitsConf. (ISSCC) Dig. Tech. Papers, Feb. 2002, pp. 276–504.

[8]. H. Partovi et al., "Flow-through latch and edge-triggeredflip-flop hybrid elements," IEEE Int. Solid-State Circuits Conf.(ISSCC) Dig. Tech.Papers, pp. 138–139, Feb. 1996.

[9]. E. Consoli, M. Alioto, G. Palumbo, and J. Rabaey,"Conditionalpush-pull pulsed latch with 726 fJops energy delayproduct in 65 nmCMOS," in IEEE Int. Solid-State CircuitsConf. (ISSCC) Dig. Tech.Papers, Feb. 2012, pp. 482–483.

[10]. V. Stojanovic and V. Oklobdzija, "Comparative analysis of masterslavelatches and flip-flops for high-performance and low-power systems,"*IEEE J. Solid-State Circuits*, vol. 34, no. 4, pp. 536–548, Apr.1999.

