COMPARATIVE STUDY AND DESIGN A CMOS CURRENT MIRROR TOPOLOGIES FOR LOW POWER APPLICATION

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Abstract: The Current mirrors are the core structure for almost all analog and mixed mode circuits. The performance of the analog structures depends on the performance of current mirror, which largely depends on their characteristics. Low voltage design circuit, low voltage currents mirrors are mandatory with high performance. In this paper, first we study simple current mirror and literature available Low voltage cascode current mirror. Second we study for low In this paper we present a comparative study for high performance current mirror for low voltage applications and cascode current mirror topology are designs Tanner EDA tool in S.edit and design schematic is simulated using T-SPICE simulator 0.18µm technology with power supply 1.0 V.

Keywords: Simple current mirror, Register biasing cascode current mirror, Linear-region transistor biasing of cascode transistors

I. INTRODUCTION

With the rapid growth of portable consumer electronics, computers and communications, more and more chips are required to have small size, low power and wide dynamic range. So, low power and low voltage analog and mixed mode circuits are gaining importance. For a low voltage and high performance analog and mixed mode circuit design current mode design technique is a better choice **[6]**. In current mode circuit design the designer have more concern with the current levels for the operation of circuit. In the current mode circuit design the current mirrors are the core structure for almost all analog and mixed mode circuits. The performance of the analog circuit depends on the performance of current mirror, which largely depends on their characteristics. There are three major sources of power dissipation in a CMOS circuit. Those are switching power, short circuit power and leakage power. Switching power is due to the charging and discharging capacitors driven by the circuit. Short circuit power is caused by the short circuit currents that arise when pairs of PMOS/NMOS transistors are conducting simultaneously. Finally, Leakage power is originates from substrate injection and sub threshold effects. One of the main reasons causing the leakage power increase is the increase of sub threshold leakage power. When technology feature size scales down, supply voltage and threshold voltage also scale down. Sub threshold leakage power increase.The current mirror (cm) is one of most common building blocks both in analog and mixed mode VLSI circuit. Current mirror is a core structure for all most all analog and mixed circuit determines the performance of analog structures, which largely depends on their characteristics. The design philosophy of analog circuits is now moving towards implementing them in the form of standard building blocks, called analog signal processing (ASP) rather than the desecrate circuits. The ASP cells ,which consists of several basic analog circuit structures and have voltage mode or current mode circuits are described as the circuits whose input and output signal are currents and their complete circuit function are described through the current signal rather than the voltage signals. The analog signal processing deal with converting signals from one analog domain to another. The basic building blocks generally use more than transistor and perform only one function. Current mirror is an essential structure or circuit in most of the analog circuit applications like oscillator ,operational amplifier, voltage regulator, analog memory design, VLSI test circuit and current conveyor.[2]

II. SIMPLE CURRENT MIRROR

A basic current mirror is shown in figure 1. It is composed of two transistors, of which one, M1is diode-connected. M1 receives the reference current Iref and measures it by developing at its gate the voltage VGS1 this voltage biases the gate of M2.Figure 1shows a basic two transistor NMOS current source. The drain and source terminals of the enhanced-mode transistor M1 are connected, which means that M1always biased in the saturation region because a MOS transistor behaves as a small signal resistor when gate and drain are shorted. A transistor in this configuration is referred to as "diode – connected" transistor. The device is always in saturation. Assuming λ =0, we can write the reference current as

$$I_{REF} = K_{n1}(V_{GS} - V_t)^2 \qquad (1)$$

Solving for V_{GS} yields

$$V_{GS} = V_{t1} + \sqrt{\frac{I_{REF}}{K_{n1}}} \qquad (2)$$

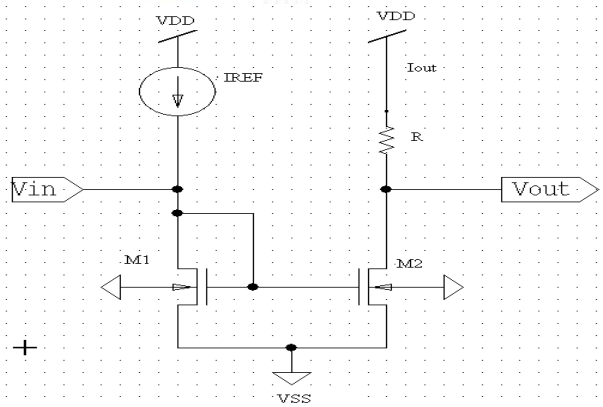

Figure 1 Simple current mirror.

The drain current to be independent of the drain current to source voltage transistor M2 should be biased in the saturation region .the load current is

$$I_0 = K_{n2}(V_{GS} - V_{t2})^2 \quad (3)$$

Substituting equation (1) and (2)

$$I_0 = K_{n2}\left[\sqrt{\frac{I_{REF}}{K_{n1}}} + V_{t1} - V_{t2}\right]^2 \quad (4)$$

If M1 and M2 are identical transistor, then Vtn_1=Vtn_2 and kn_1 = kn_2, and equation (4) becomes

$$I_0 = I_{REF} \quad (5)$$

There is no gate current source in MOSFETS the induced load current is identical to the reference current provided the two transistors are matched. The relationship between the load current and the reference current changes. If the width – to- length ratios, or aspect ratio, of the two transistors changes. If the transistors are matched except for the aspect ratios, we find, $I_0 = \frac{(W/L)_2}{(W/L)_2} I_{REF}$ The ratio between the load and reference current is directly proportional to the aspect ratio and gives designers versatility in their circuit designs.

III. LOW VOLTAGE CURRENT MRROR TOPOLOGY

A .Level shifted low voltage current mirror

Figure 2 shown the level shifted low voltage cascode current mirror it is the combination of conventional low voltage and level shifted current mirror. The combined the low voltage and level shifted current mirror present a level shifted low voltage current mirror. In this current mirror topology to achieve larger dynamic range for low voltage operation. Level shifted low voltage current mirror construct five transistor M1,M2,M3,M4 and M5 where M1,M2,M3,M4 are NMOS and M5 is PMOS transistor.The operation of M5 and M3 are similar in the figure 2 of M 5 and M1 we adopt the same assumptions in low voltage in this current mirror. We assume figure 2 the threshold voltage of M5 is V_{tp} , when the level shifted current mirror transistor M5 and M1 on must be conditions satisfied $V_{GS3} > V_{tn}$ and $V_{GS5} > V_{tp}$, but when $V_{tp} > V_{tn}$ there is a difficulty to the condition satisfy $V_{DS3} > 0$ wide range of input current Iin2.We literature survey we can find the most suitable operation mode of M5 is sub threshold region because here low input current and in saturation region high input current of M1 and M3. The assumption under the $V_{SD5} > 3V_t$,the sub-threshold drain current of transistor M5 can be expressed by

$$I_{bias\,2} \approx \frac{W_5}{L_5} I_{DO5} \exp\left(\frac{V_{SG5} - |V_{tp}|}{nV_T}\right) \quad (6)$$

In above equation (6) W5 and L5 represent the channel width and length of transistor M5, and V_T (approximately ≈26mv at room temperature) [2] is thermal voltage. The Constant n and I_{DO5} are process parameters. Typically value of $I_{DO5} \approx 20nA$ and n lie between 1.2 and 2.0 [2]. For the sub-threshold operation of transistor M5 ($V_{SG5} \approx |V_{tp}|$) and saturation operation of transistor M1 and M3, find

$$I_{in2} \le \frac{kA_C V_{SG5}^2}{2} \le \frac{kA_C V_{tn}^2}{2} \quad (7)$$

$$V_{tn} \le V_{in2} \le V_{SG5}\sqrt{\frac{A_C}{A_M}} + V_{tn} \le V_{tn}\left(1 + \sqrt{\frac{A_C}{A_M}}\right) \quad (8)$$

When transistors M1, M3, M5 are in sub-threshold region, and the gate to source voltage of M1, M3 and M5 are almost near to their threshold voltages, can find

$$I_{in2} \le \frac{I_{DO1} W_1}{L_1} \quad (9)$$

$$V_{in2} = nV_T \ln \frac{I_{in2}}{I_{DO1}} \frac{L_1}{W_1} + V_{tn} \le V_{tn} \quad (10)$$

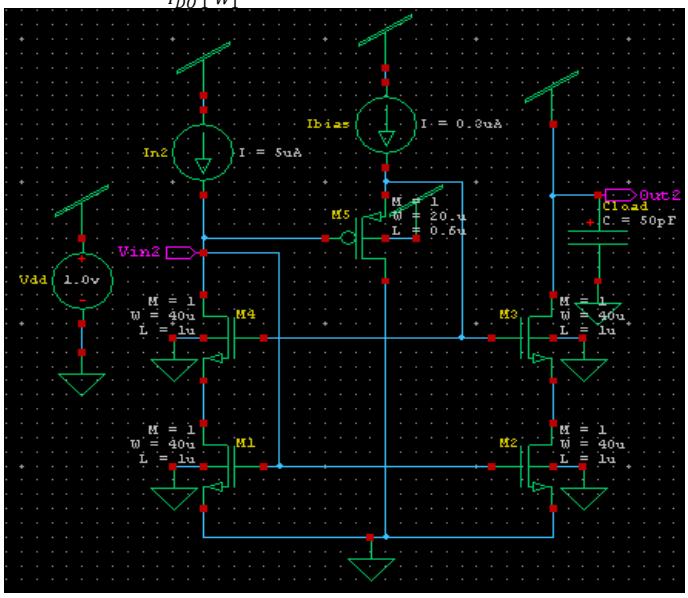

Figure 2: Level Shifted Low Voltage Cascode Current Mirror

Sub threshold operation of transistor M5, when the input current Iin2 increases input voltage Vin2 increases, transistor M5 shifts the voltage level at gate terminal of M3, there for this current mirror improved the upper limit of the input current, compared to conventional low voltage cascode current mirror. The current through M5 should be small enough to keep in transistor M5 in sub-threshold region. Correspondingly channel width and length ratio of transistor M5 should also be large. The current through M1 and M3 should be large to keep it in saturation region. Level shifted low voltage cascode current mirror input current Iin2 is low, transistor M1 and M3 are operate in sub-threshold region. When input current (i.e. Iin2) is low, M3 and M1 will operate in sub- threshold region. If only M5 operates in sub-threshold region and M1-M4 are restricted to operate in saturation region, this CM will possesses better frequency response and the lower limit of the input current.

B. Register biasing of cascode transister

As shown in Figure 3 a resister biasing cascode current mirror for transistor are used all four transistor M1,M2,M3 and M4 are NMOS transistor .in figure a register in series with input node and produce biase voltage of Transistor of M1 and M3 [12]. In this structure increase input current range but integrated register suffer from process variation because this architecture gate terminal voltage not precise. In case the register value decreased as input current rise further.

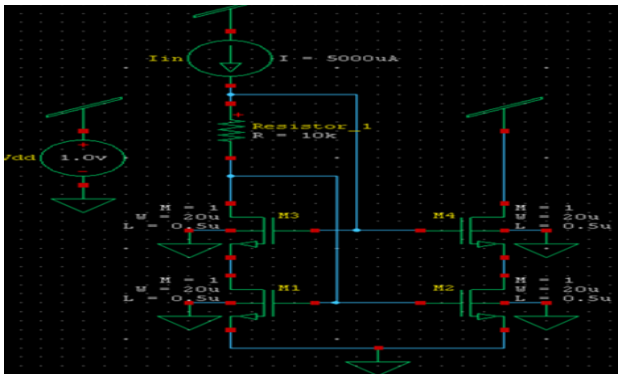

Figure 3 Register Biasing of Cascode Transistors[7]

A selection of gate source voltage conditions for a specified range of input currents can be achieved if the cascode transistor gate voltage can be made to increase with increasing input current. If the cascode transistor should be biased to condition $V_{ds1} = V_{gs1} - V_t$ at all values of input current the cascode bias voltage should be

$$V_{bc} = V_T + \frac{1+N}{N}\sqrt{\left(\frac{2I_{in}}{K'}\right)} \quad (5)$$

In above equation ensure the generate bias is a replica of the input current and use this to bias the cascode as shown in Figure 3 and use the voltage generated across this resistor as the difference between the mirror transistor gate voltage and the cascode transistor gate voltage. This implementation does not satisfy the nonlinear relation but it does lead to an increase in the input current range and a useful effective input gate-source voltage in excess of the value, it requires that an input resistor in the appropriate range of values can be implemented either as a diffused resistor or as a poly resistor. Also, there is a requirement for matching between the resistor parameters (sheet resistivity) and the transistor transconductance parameter, and this is a problem, especially for poly resistors. A variation of the approach in Figure 3 is to use a transistor operating in the linear region as a resistor.. This is achieved if the gate voltage of the linear-region MOS transistor increases with the input current.

C. Linear-region transistor biasing of cascode transistors

Shown in Figure 4 a linear-region MOS transistor as resistor is used in this structure which its gate is connected to the input and value of the resistor can be changed by input current. In passing, it can be mentioned that the circuit of Figure 4 is easily extended to provide bias voltages for cascode current mirrors with more transistors in the cascode . Transistor M5 just has to be split into an appropriate number of transistors in order to create more taps on the voltage divider string transistor M5, M6. The voltage divider transistor M5, M6 analyzed by first calculating the gate-source voltage of M5 when M5, M6 is considered as a single transistor with an effective aspect ratio. The drain-source voltage of M5 is found using the Shichman- Hodges drain current relation for the linear region

$$V_{dS5} = \sqrt{\left(\frac{2I_{in}}{K'AB}\right)}\left(1 - \sqrt{\frac{AB}{A6}}\right) \quad (11)$$

From we find

$$N = \sqrt{\frac{AM}{AB}} - \sqrt{\frac{AB}{A6}} \quad (12)$$

In order to minimize the input voltage it is advantageous to select a large value of A6. As an example, for N = 1 and A6 = 4AM we find A5 = $\frac{AM}{2}$Thus, the circuit shown in Figure 4 provides almost ideal biasing conditions for the cascode transistors. This is achieved at the expense of an input voltage to the current mirror which is

$$V_{in} = V_{gs1} + V_{gs5} = 2V_t + \sqrt{\left(\frac{2I_{in}}{K'}\right)}\left(\frac{1}{A_m} + \frac{1}{AB}\right) \quad (13)$$

and this value is about twice the value found in the original low voltage cascode mirror. It is, however, comparable to the input voltage of a conventional cascode current mirror. For the adaptive bias current mirror we find the minimum output voltage given by

$$V_{outmin} = V_B - V_t = \frac{1+N}{N}\sqrt{\left(\frac{2I_{in}}{K'}\right)} \quad (14)$$

In contrast to the fixed bias current mirror, this minimum output voltage is dependent on the input current, decreasing with decreasing input current.

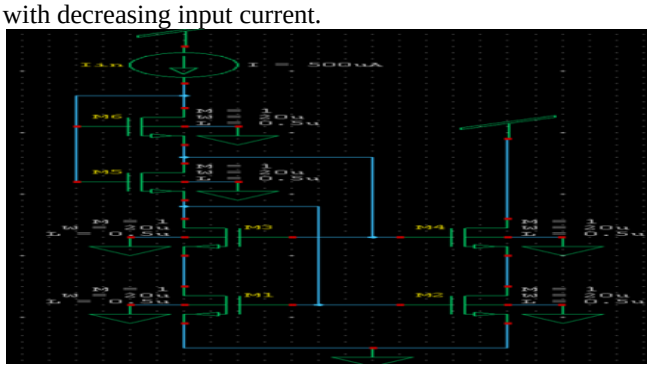

Figure 4: Linear-region transistor biasing of cascode transistors[7]

D. Proposed low voltage cascode current mirror[7]

The proposed [7] low voltage current mirror architecture shown in figure 5 five transistor are used four transistor M1, M2,M3 and M4 are NMOS transistor and Transistor M5 is PMOS transistor. In this circuit PMOS transistor M5 create a biase voltage for cascade transistor M3 and M4 for proposed low voltage cascade current mirror in this architecture body effect is removed by connecting source to body terminal of transistor of M5 for minimize input voltage requirement. In this structure ensure the transistor M1 and M3 operate in saturation region, the Vin should be

$$V_{in} = V_{SG5} + V_{ov1} = V_{ov1} + V_{th} + V_{ov3} + V_{ov1} \quad (15)$$

Where in equation V_{ov1} and V_{ov3} are overdrive voltage of transistors M1 and M3 respectively.

$$V_{ov1} = \sqrt{\frac{2I_{in}}{K'A_1}} \quad (16)$$

$$V_{ov3} = \sqrt{\frac{2I_{in}}{K'A_3}} \quad (17)$$

Where $A_1 = \frac{W_1}{L_1}, A_3 = \frac{W_1}{L_1}$ and *W3, L3* are width and length of transistor M3 respectively

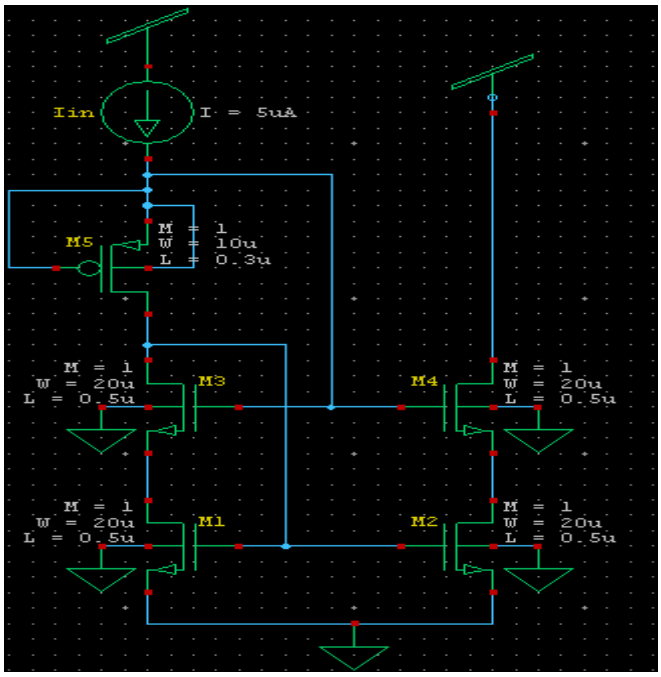

Figure 5: Proposed voltage cascode current mirror.[7]

Adaptive based low voltage current mirror are assumed all transistor are identical and body effected ignored and threshold voltage of current mirror Vth and transcunctance parameter *K'=Cox.*

The input voltage and input current can be found by replacing equations (16) and (17) in (15).

$$V_{in} = V_{th} + 2V_{od} = V_{th} + \sqrt{\left(\frac{2I_{in}}{K'}\right)}\left(\frac{1}{A_1} + \frac{1}{A_3}\right) \quad (18)$$

$$I_{in,min} = \frac{K'(V_{in} - V_{th})^2}{2\left[\frac{1}{\sqrt{A_1}} + \frac{1}{\sqrt{A_3}}\right]^2} \quad (19)$$

From above equations, in *Vin* and input current *Iin* that leads to the self-biasing Cascode Current Mirror configuration and larger upper limit. Because all input current/voltage changes will transfer to the cascode transistors through M5. This circuit has a very larger upper limit input current (*Iin,max*) and small value of current gain error rate compare to convention current mirrors

IV. SIMULATION RESULT

The presented cascode current mirror topology circuits are simulated at standard 0.18µm CMOS technology with power supply 1.0 V. Cascode Current mirror performnce comparison shown in table I.

Current transfer characteristics of register biasing cascade transistor current mirror

Figure 6 shows current transfer characteristics of Register biasing Cascode Transistor Current mirror for 0.18µm IBM MOS technology parameters. Drain current id (M3) of transistor M3 is input or reference current and drain current id(M4) of transistor M4 is the output current. From simulated waveform, it is very clear that output current very closely tracks the input or reference current.

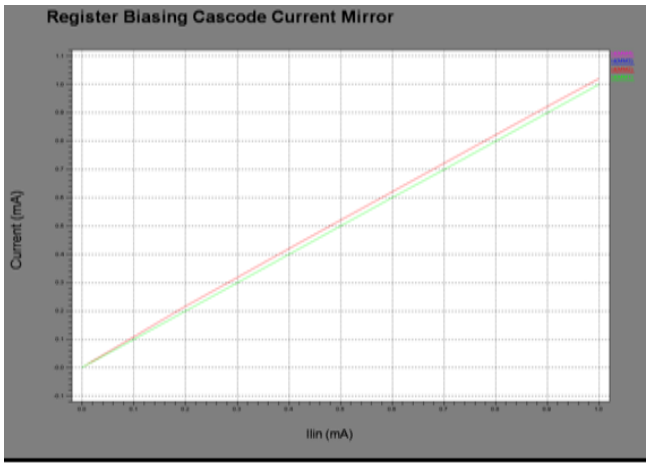

Figure 6 Current transfer characteristics Register biasing Cascode Transistor Current mirror

Input characteristics of Register biasing Cascode Transistor CM

Figure 7 shows the input characteristics of Register biasing Cascode Transistor Current mirror as shown in figure 3Input voltage (Vin) is plotted by sweeping input current from 0 µA to 1 mA by using 0.18µm IBM MOS technology model parameters.

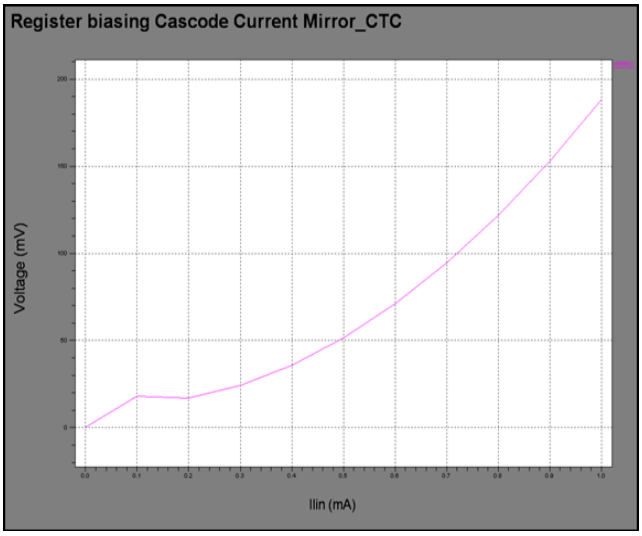

Figure7: Input Characteristics of Register biasing Cascode Transistor Current mirror

Power Dissipation Results for Register biasing Cascode Transistor Current mirror

Register biasing Cascode Transistor Current mirror circuit is simulated using 0.18µm IBM MOS model parameters with supply voltage 1.0 V and I_{in} of 400µA. Width and length of transistors (M3 & M4 and M1 & M2) are kept same. Transient analysis is used to calculate the power dissipation in the current mirror. Figure 8 shows power dissipation results. Power results are reported at the end of transient simulation in the output file

VVdd from time 0 to 2e-007
Average power consumed -> 5.225319e-003 watts
Max power 5.475648e-003 at time 5.25e-009
Min power 4.990006e-003 at time 6.25e-011

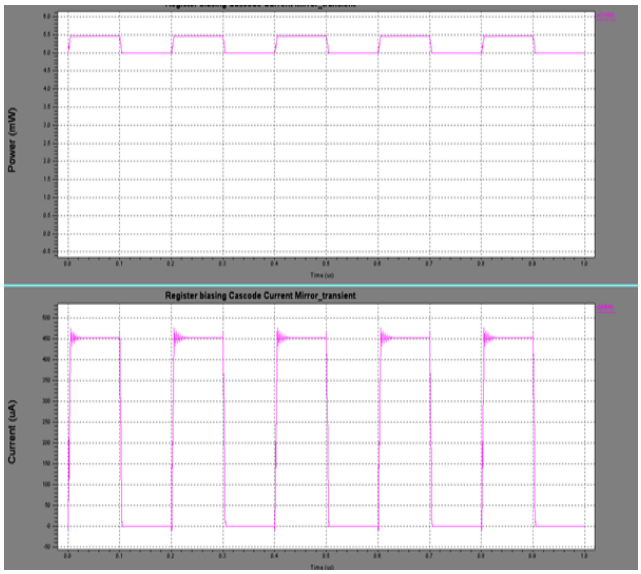

Figure 8: Power dissipation result for Register biasing Cascode Transistor Current mirror

Frequency Response of Register biasing Cascode Transistor CM

The frequency response of Register biasing Cascode Transistor Current mirror is shown in figure 9 The frequency response of cascode current mirror is dependent on the capacitive load (Cload). In figure 3 the -3db banwidth is 31.13MHz for a load capacitance of 5 pF.

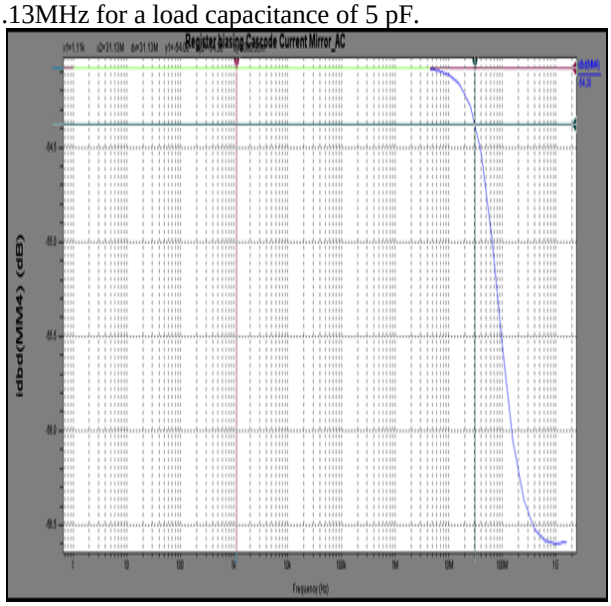

Figure 9 Bandwidth of Register biasing Cascode Transistor Current mirror

Simulation Results & Waveforms of of Linear Region transistor biasing of cascode transistor current mirror Current Transfer Characteristics of Linear Region transistor biasing of cascode transistor CM

Figure 10 shows current transfer characteristics of simple current mirror for 0.18µm IBM MOS technology parameters. Source current is (M6) of transistor M6 is input or reference current and drain current is (M4) of transistor M4 is the output current. From simulated waveform, it is very clear that output current very closely tracks the input or reference current.

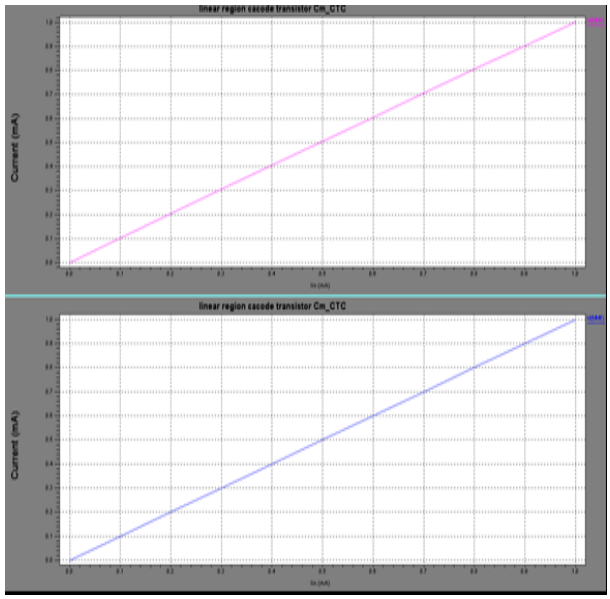

Figure 10 Current transfer Linear Region transistor biasing of cascode transistor CM

Input Characteristics of Linear Region transistor biasing of cascode transistor current mirror

The input characteristics of Linear Region transistor biasing of cascode transistor CM as shown in figure 11 Input voltage (Vin) is plotted by sweeping input current from 0 µA to 1mA by using 0.18µm IBM MOS technology model parameters.

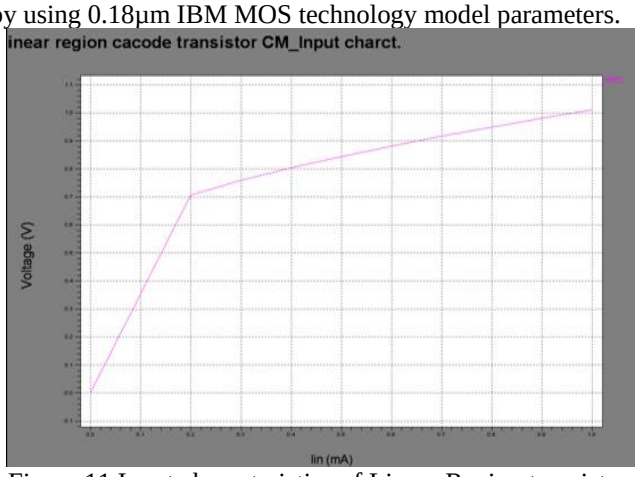

Figure 11 Input characteristics of Linear Region transistor biasing of cascode transistor CM

Power dissipation for Linear Region transistor biasing of cascode transistor current mirror

Linear Region transistor biasing of cascode transistor CM circuit is simulated using 0.18µm IBM MOS model parameters with supply voltage 1.0 V and I_{in} of 5.5mA. Transient analysis is used to calculate the power dissipation in the current mirror. Figure 12 shows power dissipation results. Power results are reported at the end of transient simulation in the output file .

Power Results

VVdd from time 1e-009 to 1e-006

Average power consumed -> 2.984061e-003 watts

Max power 5.518074e-003 at time 7.25e-009

Min power 4.984553e-004 at time 2.0025e-007

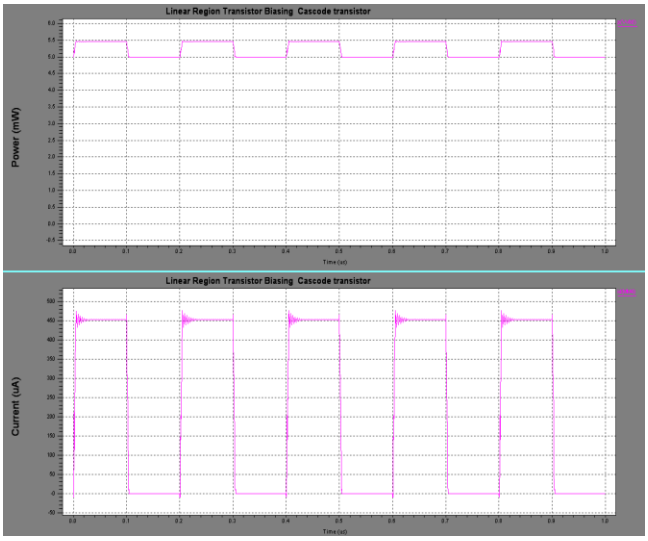

Figure 12: Power dissipation for Linear Region transistor biasing of cascode transistor CM

Frequency Response of Linear Region transistor biasing of cascode transistor current mirror

The frequency response of Linear Region transistor biasing of cascode transistor current mirror is shown in figure 15. The frequency response of cascode current mirror is dependent on the capacitive load (Cload). In figure 13 the -3db banwidth is 1.23GHZ for a load capacitance of 50 pF.

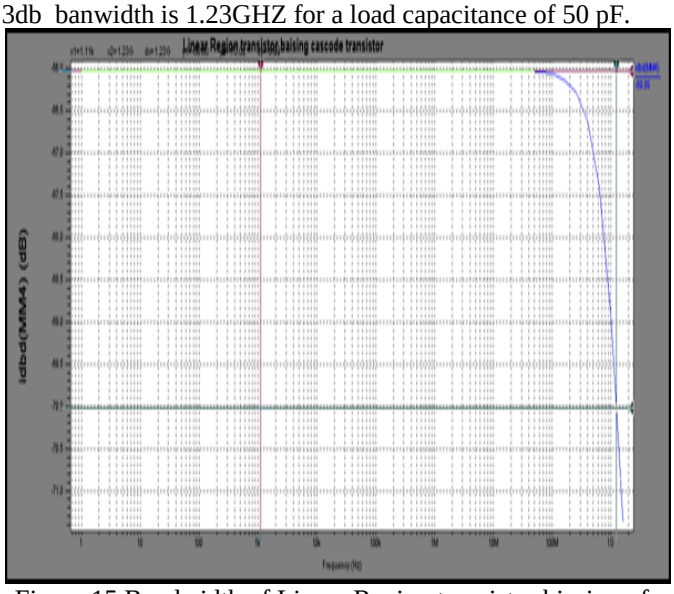

Figure 15 Bandwidth of Linear Region transistor biasing of cascode transistor CM

Simulation Result & waveform of Proposed low voltage Cascode Current Mirror

Input Characteristics of Proposed low voltage Cascode Current Mirror

Figure 14 shows the input characteristics of Register biasing Cascode Transistor Current mirror Input voltage (Vin) is plotted by sweeping input current from 0 µA to 1 mA by using 0.18µm IBM MOS technology model parameters.

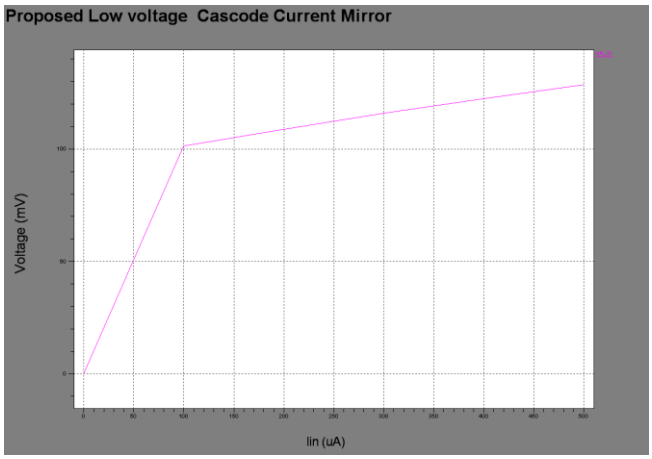

Figure 14 Input Characteristics of Proposed low voltage Cascode Current Mirror

Current Transfer Characteristics of Proposed low voltage Cascode Current Mirror

Figure 17 shows current transfer characteristics of cascode current mirror for 0.18µm IBM MOS technology parameters. Source current is (M5) of transistor M5 is input or reference current and drain current id(M4) of transistor M4 is the output current. From simulated waveform, it is very clear that output current very closely tracks the input or reference current.

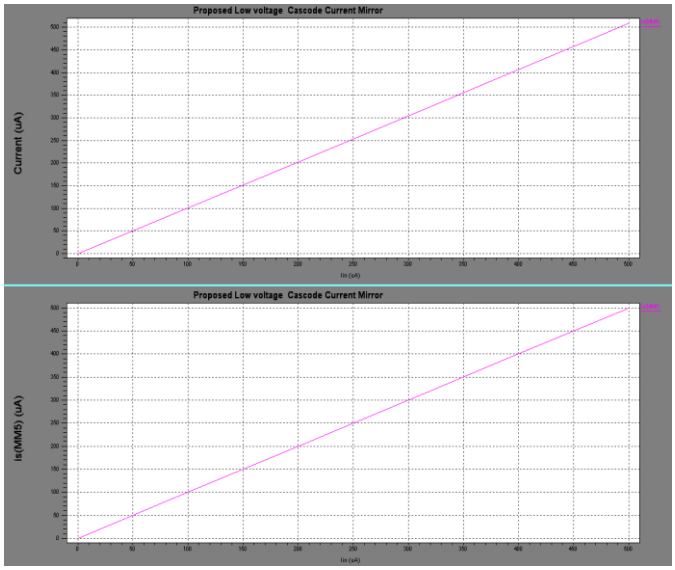

Figure 15 Current transfer Characteristics of Proposed low voltage Cascode Current Mirror

Frequency response for proposed low voltage Cascode Current Mirror

The frequency response of Cascode current mirror is shown in figure 16. The frequency response of cascode current mirror is dependent on the capacitive load (Cload). In figure 16 the -3db banwidth is 1.28GHZ for a load capacitance of 50 pF.

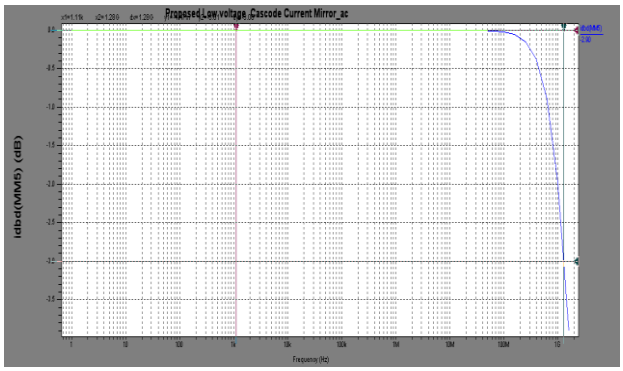

Figure 16 Bandwidth of proposed low voltage Cascode Current Mirror

Power dissipation for proposed low voltage Cascode Current Mirror

Proposed low voltage cascade current mirror circuit is simulated using 0.18µm IBM MOS model parameters with supply voltage 1.0 V and I_{in} of 4.5mA. Transient analysis is used to calculate the power dissipation in the current mirror. Figure 20 shows power dissipation results. Power results are reported at the end of transient simulation in the output file .

Power Results

Vdd from time 0 to 2e-007

Average power consumed -> 2.762923e-003 watts

Max power 5.077224e-003 at time 7.25e-009

Min power 4.783021e-004 at time 6.25e-011

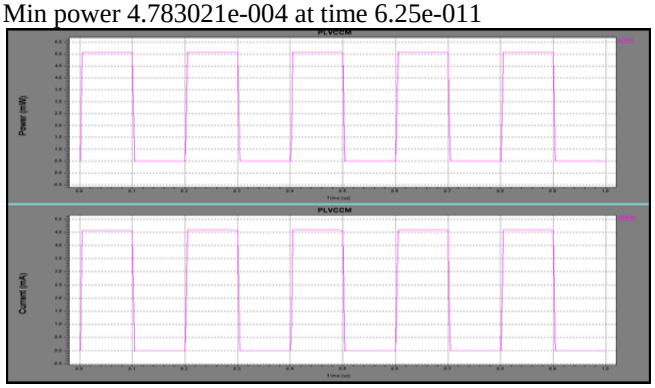

Figure:17 Power dissipation for Proposed low voltage Cascode Current Mirror

Table I CM topology performance comparison

Specification	RBCTCM	LRCCM	PLVCM
Power supply	1.0	1.0	1.0
Power dissipation	522mw	298mw	276mw
Bandwidth	31.13Mhz	1.23Ghz	1.28Ghz

V. CONCLUSION

The current mirror circuit is the main bottleneck in analog circuit design like voltage regulator, oscillator, and operational amplifier, current conveyor, memory. In this paper we study simple current mirror, low voltage current mirror and Comparative study of literature available three current mirror topology design and analysis of three CM topology power consumption and bandwidth with 1 volt power supply. In this paper we present performance comparison of three current mirror topology performance, PLVCM [7] is more suitable for low power analog design circuit compare to other two RBCTCM and LRCCM.

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