STABILITY ANALYSIS OF 8T-SRAM CELLAT ULTRA LOW VOLTAGE

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Abstract: This paper represents the stability analysis of 8T-SRAM cell by calculation of Static Noise Margin (SNM) using butterfly curve(1V, 0.6V) of voltage supply to the cell. Additionally we have used N-curve metrics for better analysis of Write ability with metrics (WTV, WTI), Read stability with metrics (SVNM, SINM) which are given by I-V characteristics of SRAM cell. These N-curve metrics are compared and tabulated for range of supply voltages from 0.4V to 1V.Simulations are done under 45nm CMOS technology using CADENCE VIRTUOSO, MATLAB.
Keywords: SNM, SVNM, SINM, WTI, WTV, SRAM.

I. INTRODUCTION

Static Random Access Memory (SRAM) and Dynamic Random Access Memory (DRAM) are used in portable devices like Computers, Mobile Phones for holding the data. Though SRAM requires more transistors than DRAM for holding the data, DRAM has a drawback of extra circuitry that is required for refreshing DRAM to hold the data. SRAM exhibits data remanence unless the power supply to the cell is shut off without any extra circuitry required for refreshing the SRAM, this is an advantage for which SRAM is used in Cache memory.Massive use of SRAM cell in System on Chips (SoCs) for cache memory is due to its high performance, low power consumption and high stability. Rapid scaling of CMOS technology leads to uncertainties in parameters like cell stability, leakage current, power consumption and cell area. SRAM cell stability at ultralow voltages is the major concern in our discussion. Conventional method for stability analysis is done by plotting voltage Transfer Characteristics (VTC) of SRAM cell for each Hold, Read and Write operations [1-2]. After obtaining VTC's Static Noise Margin (SNM) is estimatedwhich has a drawback of in depth analysis for cell stability. Very few papers have been published related work on alternate method for stability analysis of SRAM cell. Analysis of cell stability by alternative method is done with N-curve metrics. N-curve metrics contains combined information about voltage and current for both read and write operations [3-4]. In this paper we have analyzed stability of 8T-SRAM cell with SNM definition by plotting butterfly curve for Hold, Read and Write operations at ultralow voltage supply [5-6-7]. Simulations are done at two different voltages 1V and 0.6V, comparison of SNM for different operations is made at these voltages. Secondly N-curve metrics are analyzed and metrics SVNM, SINM, WTV and WTIare derived [8]. These metrics are compared for range of voltages from 0.4V to 0.6V. This paper is organized as follows. In section [2] Estimating SNM of SRAM using Butterfly curve, section [3] Analysis with N-curve metrics, section [4] Comparing different metrics with the help of appended N-curve simulated data, section [5] Conclusion.

II. STABILITY ANALYSIS USING BUTTERFLY CURVE

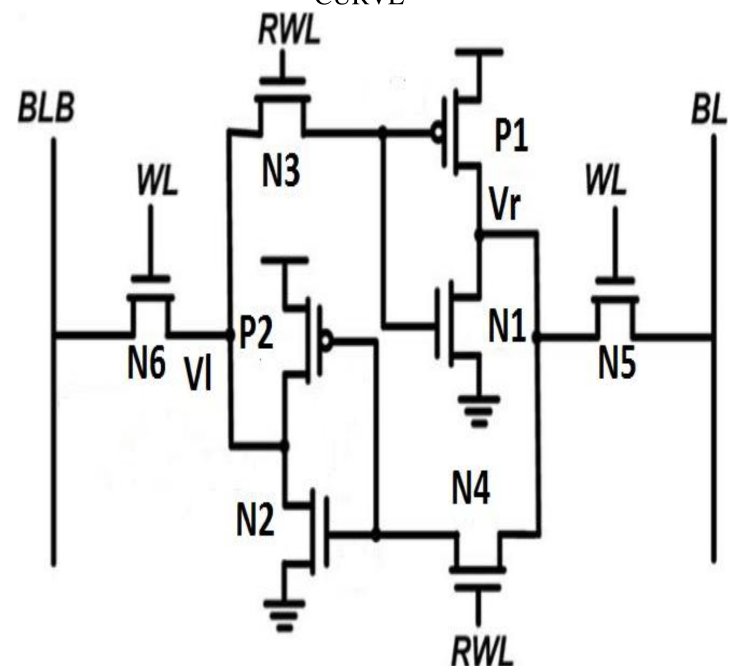

Fig1.Schematic of 8T-SRAM cell

Fig 1 shows the schematic of 8T-SRAM cell, it consists of two access transistors (N5, N6) with the help of these transistors we access the data for both Read and Write operation. The cross coupled inverters (P1, N1), (P2, N2) are used for storing one bit of information at a time either 0 or 1.N1 and N2 are driver transistors which drives current through them, in read operation to avoid flipping of data driver transistors must be 1.5-2.0 larger than access transistors N5,N6 respectively.N3 and N4 are transistors used to separate two cross coupled inverters for accessing the data bit stored, these two transistors also acts as a feedback inputs for inverters. BL and BLB are Bit Line voltages, these values are inverted (if BL is 0 then BLB is 1 vice versa), WL is Word Line voltage which is used to switch ON or OFF the access transistors depending on the operation performed, RWL is Read Word Line voltage which is used to turn ON or OFF feedback for cross coupled inverters. Static Noise Margin (SNM) is a quality term to measure stability of the cell, SNM is tolerable DC noise voltage without flipping the data. HSNM,RSNM and WSNM are definitions of SNM for

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Hold, Read and Write operations respectively which are maximum tolerable internal node voltages for non-destruction of operation. SNM for one EYE differs from another EYE, minimum of both SNM gives the actual SNM for intended operation.

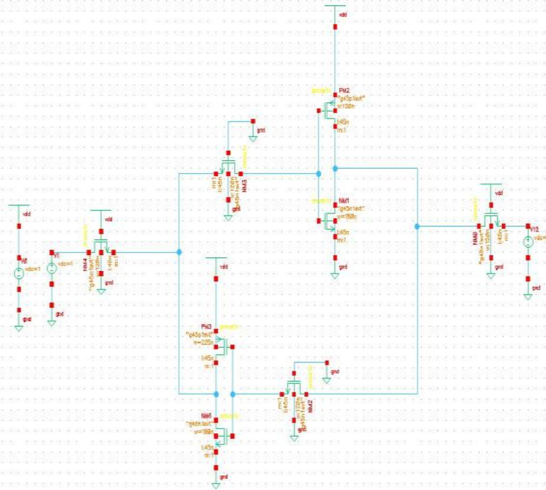

Fig 2.schematic implementation of 8T-SRAM cell in CADENCE VIRTUOSO at 45nm CMOS Technology.

A. SNM FOR HOLD OPERATION(HSNM)

For Hold operation to be perfromed access transistors (N5, N6) are turned OFF,BL and BLB are swept from Vdd to 0.RWL is turned ON and kept at Vdd, WL is turned OFF which will turn OFF both access transistors.By plotting VTC of internal voltages Vr and Vl Butterfly curve for Hold operation is derived.Placing the maximum square between the eyes of the Butterfly curve determines the DC noise tolerable voltage,HSNM is given by minimum of SNM1,SNM2.Fig3 shows the Butterfly curve for Hold operation at 1v of power supply to the cell(Vdd).fig4 shows Butterfly curve at 0.6v of power supply to the cell(Vdd).HSNM variation at ultralow voltages(1V, 0.6V) is compared and tabulated at Table 1.

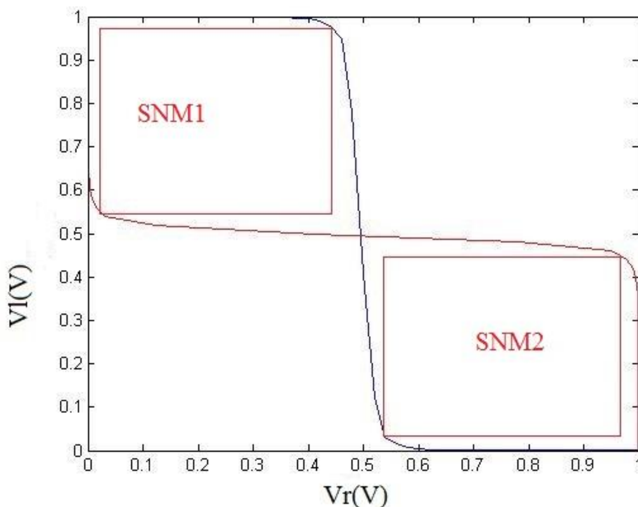

Fig3.Butterfly curve for Hold operation at 1Vsupply to SRAM cell.

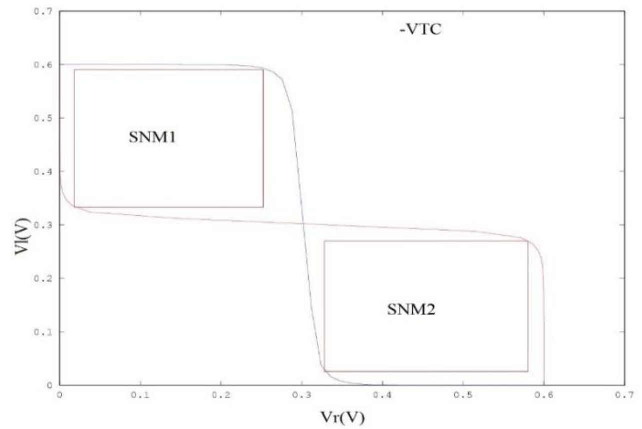

Fig 4.Butterfly curve for Hold operation at 0.6V voltageto supply to SRAM cell.

B. SNM FOR READ OPERATION(RSNM)

Succesful Read operation is performed by accessing the contents stored in inverters without flipping the data. Access transistors are turned ON by suppling WL with Vdd, BL and BLB are pre-charged to Vdd, RWL is turned OFF, since transistors N3 and N4 are turned OFF contents of inverters are accessed saperately. Read operation is of two types either 0 or 1 which is decided depending on wheter BLB discharges or holds voltage. Read is done through BLB,to Read logic -0 provided Vl is at “0” and Vr is at “1” then BLB discharges through transistors N6 and N2 to ground and for logic-1 Read operation provided Vl is at “1”and Vr is at “0” BLB holds its charge.For better Read operation the driver transistors strength should be 3 times the access transistors strength,else W/L ratios of driver transistors should be greater than that of access transistors.fig5 shows Butterfly curve for 1V of voltage supply,Fig6 at 0.6V of voltage supply to the cell.

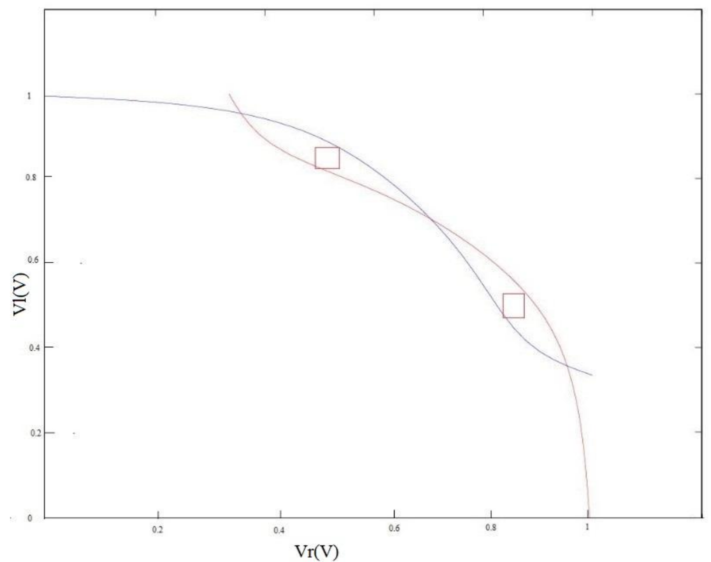

Fig 5.Butterflycurve for Read operation at 1V voltage supply to cell.

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Fig 6.Butterfly curve for Read operation at 0.6V voltage supply to the cell.

C. SNM FOR WRITE OPERATION(WSNM)

Fig 7.Halfcell schematic implementation of SRAM cell for write operation.

During write operation of SRAM cell two signals BL, BLB are kept at different voltage levels one at Vdd and the other at 0.BL is the input to N5 and BLB is the input to N6 transistor. Simultaneously WL goes high(Vdd) which helps to written the data into the SRAM cell by accessing transistors. RWL is kept at Vdd so that N3 and N4 transistors acts as feedback to connect two inverters. To perform Write operation of logic-1, BL is kept at voltage Vdd and BLB at 0 charge from BL will be discharged through N5 and N1 this will change the data stored in inverter from logic-0 to logic-1 provided Vr is at logic-0.For performing Write operation of logic-0, BL is kept at 0 and BLB at Vdd. The data stored in inverter discharges through N1 and N5 to BL, changing the content from logic-1 to logic-0, providedVr is at logic-1.WSNM is measured with the half cells of SRAM cell as shown in Fig7.WSNM is a measure of ability of an SRAM cell to pull down the node voltage which store logic-1 to a voltage which is less than the switching threshold voltage of the inverters which store logic-0 or vice versa. In this paper we have analyzed WSNM at voltages (0.6V, 1V) of supply to the cell. Fig8 shows Butterfly curve for Write operation at 1V of voltage supply to the cell. Fig9 shows Butterfly curve for Write operation at 0.6V of voltage supply to the cell.

Fig 8.Butterfly curve For WRITE SNM at 1V.

Fig 9.Butterfly curve For WRITE SNM at 0.6V.

Table1. Comparison of SNM for cell at 1V and 0.6V.

SNM	At 1V	At 0.6V
HOLD	421mV	278mV
READ	197mV	108mV
WRITE	378mV	247mV

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III. STABILITY ANALYSIS WITH N-CURVE METRICS.

Inability of Butterfly curve to derive SINM automatically without mathematical manipulation is a drawback, Alternative method for stability analysis is done using N-curve. Complete functional analysis of SRAM cell is given by combined voltage and current metrics which are derived from N-curve. These metrics allow to overcome the limitations imposed on Vdd for SNM. Both Read stability and Write ability are measured using N-curve in one simulation.

A. EXTRACTION OF N-CURVE METRICS

To extract N-curve both BL and BLB are clamped at Vdd, WL is turned ON and RWL is turned ON.An additional voltage source Vin which sweeps from 0 to Vdd is kept at Vrinternal voltage and current Iin is measured through it. New metrics for analysis of Read stability is given by SVNM and SINM, for write ability is given by WTV and WTI.

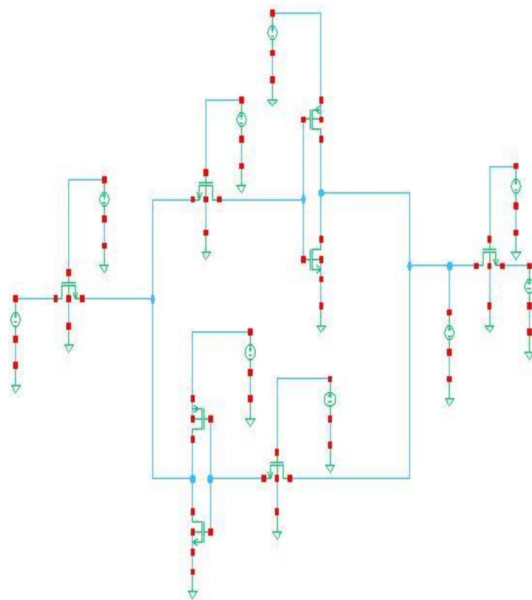

Fig 10. Schematic implementation of SRAM cell for N-curve metrics.

B. READ STABILITY ANALYSIS USING N-CURVE METRICS.

Static Voltage Noise Margin (SVNM) metric is given by the voltage difference between points A and B in N-curve shown in Fig11,it is maximum DC noise voltage that can be tolerable by internal node Vr without flipping the contents of data. Static Current Noise Margin (SINM) metric is given by current information which is the peak value between points A and B, it is maximum value of injected current that can be tolerated before the contents changes. Using these metrics we define stability both in voltage and current, for suppose if SVNM is small and SINM is large even then the cell is stable because noise current required to change contents stored is very large. In this paper we have done N-curve analysis at two different voltages (1V, 0.6V) Fig11 shows N- curve analysis at 1V and Fig12 Shows N-curve analysis at 0.6V.

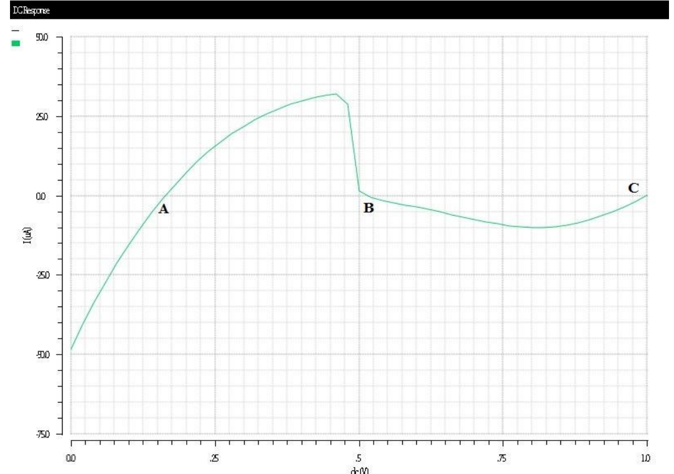

Fig 11.N-curve simulation at 1V supply to the cell.

C. WRITE ABILITY ANALYSIS USING N-CURVE METRICS.

N-curve also provide information regarding write ability of SRAM cell, voltage and current information given by simulations indicates how easy or difficult it is to do write operation. Now we analyze N-curve from points C to B where internal storage node Vr is 1.Peak voltage between C and B gives Write Trip Current (WTI) margin which is current required to Write the cell when bit-lines are at Vdd, voltage difference between points C and B gives Write Trip Voltage (WTV) margin which is voltage drop needed to flip the internal storage node “1” of SRAM cell with bit-lines kept at VDD.

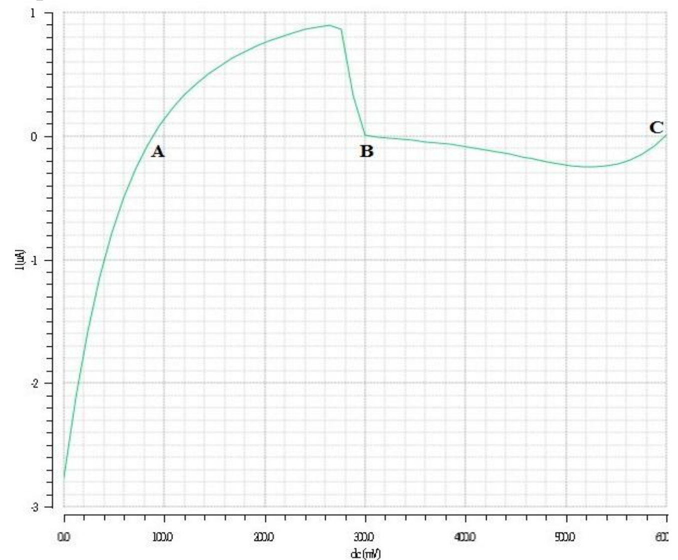

Fig 12.N-curve simulation at 0.6V supply to the cell. A, B and C are points where both current and voltage values are 0.

IV. COMPARISON OF METRICS USING APPENDED N-CURVE.

N-curve metrics are compared for a range of voltages from 0.3V to 1V, this comparison gives the information about variation of stability metrics at below sub threshold voltage supply to the cell.

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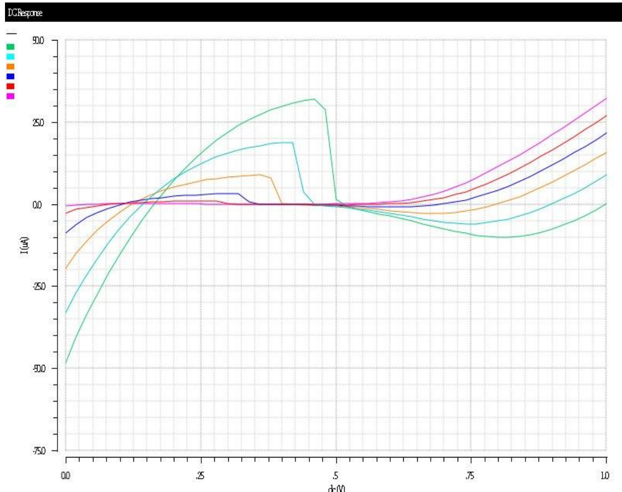

Fig 13.appended simulation of N-curve from 0.3V to 1V supply to the cell.

Table2. Comparison of N-curve metrics at different voltages.

VDD (V)	SVNM (mV)	SINM (uA)	WTV (mV)	WTI (uA)
1V	348.67	31.78	439.25	-10.20
0.9V	317.60	18.75	391.69	-6.06
0.8V	284.06	8.86	387.03	-2.85
0.7V	248.34	3.18	344.80	-0.90
0.6V	214.35	0.89	295.80	-0.25
0.5V	180.59	0.20	245.88	-0.05
0.4V	146.55	0.03	196.97	-0.008
0.3V	112.19	0.002	146.30	-0.001

V. CONCLUSION

In this paper, we have analyzed new metrics and compared with SNM for better analysis of Read stability and Write ability. It is observed that stability of the cell depends on both current and voltage information, Write Trip point information given by N-curve would be critically important for the cell design under nanometer technologies. Analysis under sub threshold voltage supply to cell gives information regarding the variation of current and voltage for stability of cell. Hence N-curve definition is better way to analysis cell compared to conventional Butterfly curve method.

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