MODELING OF MMC CONVERTER BASED ON HVDC AND TESTING BASED ON PHYSICAL CONTROL SYSTEM

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Abstract-This paper explores the operation of modularmulti-level transformers (MMC) as a means for employing the power from out- reinforcement wind power shops. The MMC consists of a large number of simple voltage sourced motor (VSC) sub modules that can be fluently assembled into a motor for high-voltage and high power. The work shows that the MMC motor has a fast response and low harmonious content in comparison with a two- position VSC option. This paper gives the modeling approach used, including a result to the modeling challenge assessed by the veritably large number of switching bias in the MMC. Real- time simulation of modular multilevel motor (MMC)- grounded. This paper describes an effective modeling approach for real- time simulation of MMC-HVDC. Taking advantages of the full resemblant armature of the field-programmable gate array (FPGA), further than 1500 submodules are suitable to be dissembled in a single FPGA The results validate the delicacy of proposed approach and real- time MMC simulator.

1. INTRODUCTION

VOLTAGE source motor (VSC)- grounded HVDC systems are of adding frequency due to the wide operation of wind power, photovoltaic power, distributed generation, and smart grid technology. Since the first VSC-HVDC design was introduced in 1990s, significant progress has been achieved in terms of adding the voltage and power standing and reducing the losses (1). These achievements are substantially due to two factors. On the one hand, rapid-fire development of power electronic bias has been furnishing the significantly increased voltage and current conditions and completely controllable switching bias similar as insulated-gate bipolar transistors (IGBTs). On the other hand, the VSC-HVDC system topology itself has been bettered. From the conventional two- position VSC ground topology, to the neutral- point clamped three- position topology, also the modular multilevel motor (MMC) topology, a variety of inquiries and testing have been conducted world wide. Most lately, MMC fashion is drawing further attention for VSC-HVDC operations (2) – (6). The advantages of MMC-grounded HVDC system are veritably straight forward. The multilevel capability produces ac voltage swells with veritably low deformation, which eliminates utmost of the filtering. The modular structure provides the inflexibility to gauge the voltage and power position by adding further sub modules (SMs). Also, compared with the traditional VSC-HVDC systems, the MMC- grounded HVDC system can reduce losses significantly due to its low frequency switching operation. The modeling of MMC faucets increases the challenge indeed more when a large number of SMs are included in a valve. On the one hand, working the large number of switching factors in a MMC valve at a small time-step is relatively time on summing. The new MMC modeling system is relatively desirable to meet the real- time simulation need for further and further ongoing MMC-grounded HVDC systems that have hundreds of SMs in a valve. On the other hand, the traditional. processor- grounded tackle, which conducts succession operations isn't suitable to handle huge quantum of data in a veritably small time- step involved in the MMC simulation. Alternately, field programmable gate arrays (FPGAs) have been proven to fluently meet this strict time- step constraint due to their essential massive resembling tackle sense coffers and full configurability (9), (10).

There have been three proposed topologies for the SM of a MMC. These topologies are partial- ground sub-module (HBSM), full- ground sub-module (FBSM) and clamp-double sub-module (CDSM) (16). The major limitation of the HBSM is that it is unable to block dc- side faults, but this can be overcome by the use of a dc- swell like the one proposed in 0. For the reasons mentioned ahead, the HBSM is named as the SM topology for the MMC. The HBSM has four possible current paths, as shown in figure 1

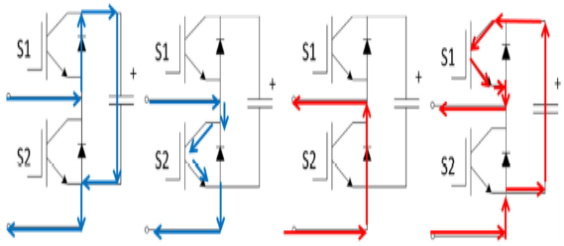

Fig. 1. Modular multilevel converter.

The MMC operates by fitting or bypassing the SM capacitor to form, in staircase shape, the affair voltage waveform (17). The capacitor is fitted when S1 is on, and bypassed when S2 is turned on. When both switches in the SM (i.e., S1 and S2) are out, the current flows through the footloose diodes. The operation of the MMC is illustrated in figure 2, using dc sources rather of capacitors and a chooser. The chooser inserts or bypasses dc sources according to the control algorithm of the MMC. The fitted dc sources produce a voltage affair with a staircase form, as shown in figure 3. The six situations voltage waveform in figure 3 is produced with five SMs per arm of the MMC.

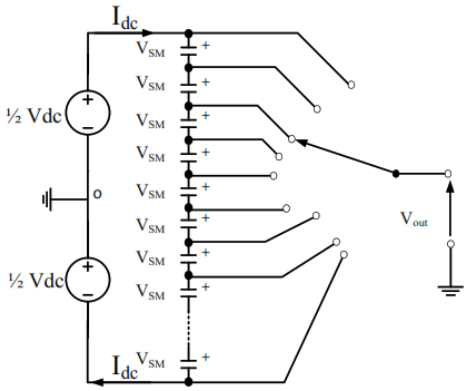

Fig. 2. MMC Representation.

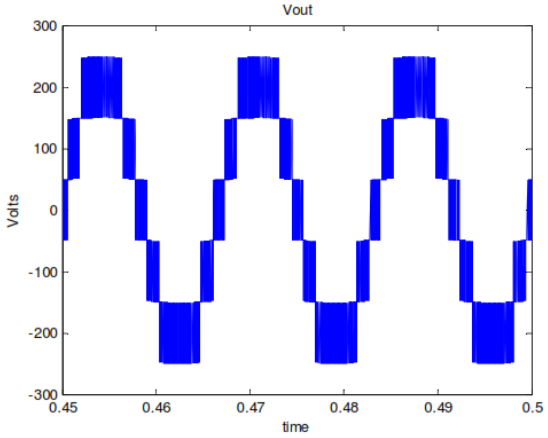

Fig. 3. Output Voltage of the MMC.

By applying Kirchhoff's voltage law to figure. 5, the arm voltage source can be defined as:

$vv_{aa1}(tt)$= 12VV_{dddd}− $vv_{aa}(tt)$= 12VV_{dddd}− vv_{aa} sin($\omega\omega 0tt$) (2)

For simplicity, (2.3) and (2.4) the relation between ac and dc variables as are defined as

mm= 32 $ıı_{aa}$ II_{dddd} (3)

kk= 2 vv_{aa} VV_{dddd} (4)

Introducing (3) and (4) into (1) and (2), respectively, gives:

$iia_{a}1(tt)$= 13II_{dddd}[1+mmsin($\omega\omega 0tt$+$\varphi\varphi$)] (5)

$vv_{aa}1(tt)$= 12VV_{dddd}[1−kksin($\omega\omega 0tt$)] (6)

In order to calculate the power in the arm of the MMC, (5) and (6) are multiplied, yielding:

$pp_{aa}1(tt)$= PP_{dddd}6[1+mmsin($\omega\omega 0tt$+$\varphi\varphi$)] [1−kksin($\omega\omega 0tt$)] (7)

PP_{dddd}=VV_{dddd} II_{dddd} (8)

Integrating (7) over half a period yields the total energy change ΔW in the arm of the MMC as follows:

Δww= 2 PP_{dddd} 3 kk $\omega\omega 0$cos$\varphi\varphi$ 1− kk cos$\varphi\varphi$2 2 32 (9)

In order to obtain the energy change of the MMC SM, (9) is divided by the number of SMs per arm (N), yielding:

$\Delta WSSSS$= 2 PP_{dddd} 3 kk $\omega\omega 0$N cos$\varphi\varphi$ 1− kk cos$\varphi\varphi$2 2 32 (10)

The energy stored in a capacitor is defined as:

ww= 1 2$ccvv$2 (11)

II EFFICIENT TECHNIQUE FOR MODELING MMC

Principally, an MMC valve consists of a reactor and chain of exactly identical series- connected half-or full- ground SMs as illustrated in Fig. 4. The operation countries of a SM, for the half-ground topology, include 1) blocked when neither IGBT is fired. In this state the capacitor is charged through the diode during the ages of positive valve current; 2) fitted ve when IGBT 1 is fired but IGBT 2 isn't fired. This causes the SM voltage VSM = VC; and 3) bypassed when IGBT2 is fired but IGBT 1 isn't fired, which causes VSM = 0. As bandied before, the computational burden for a large number of witching rudiments is relatively high. As similar, a surrogate network fashion (11) was proposed in order to model MMCefficiently for real- time simulation. The crucial conception of the surrogate network is to use a modified topology compared with the real valve but produces the same computational results

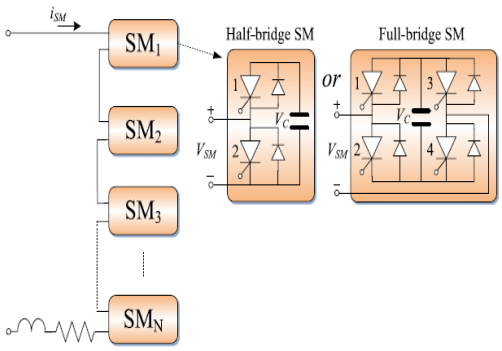

Fig. 1. MMC valve schematic diagram.

FIGURE 4 VALVE SCHEMATIC DIAGRAM

The surrogate network for a MMC valve conforming of six half- ground SMs is shown inFig. 2. The abecedarian structure block for the surrogate network is comprised of a resemblant combination of a capacitor, a discharge resistance, and an upward- directed diode, which is appertained to as a SM capacitor branch in this paper. In the SM capacitor branch, the discharge resistance mimics the discharge resistance of real capacitors.

Its value depends on the discharge time constant set by the stoner. It's also possible to enable a fast discharge resistor. The upward- directed diode tools one main specific of the real SM, which is that the individual SM capacitors can not charge to negative voltages because of the real diodes .connected across them. Fortunately, it isn't actually necessary to explicitly model the diode as a switched element in the simulation. The diode only prevents the capacitor

voltage in the SM capacitor branch from going negative. This is done by resetting negative values to zero whenever negative voltage occurs. The surrogate network, shown in Fig. 5, comprises a series connection of a reactor section, blocked SM section (diode D1, D2 and a chain of blocked SM capacitor branches), and fitted SM section (a chain of fitted ve SM capacitor branches). They passed SMs are insulated from the surrogate network and grouped into the bypassed SMs section where they discharge. The particular SMs that are contained in which section are determined in each time- step according to the blasting control input. The diodes D1 and D2 in the surrogate network apply another main specific of the MMC valve. It's that the diodes in each blocked SM always switch synchronously with the diodes in all other blocked SMs according only to the direction of the overall MMC valve current. Accordingly, it isn't necessary for every blocked SM to have a separate brace of diodes. D1 and D2 are sufficient to assure that the overall MMC valve current causes the correct harging to do in all SM capacitors in the blocked SM. However, the voltage drops across diode D1 and D2 is modeled in the surrogate network as N times the voltages drop across one, If there are N SMs in a valve.

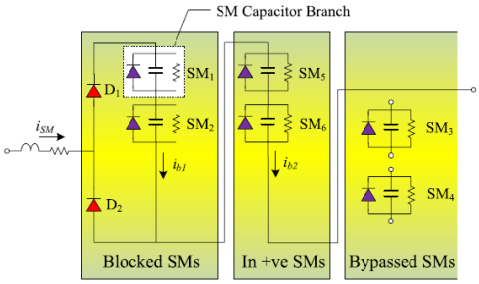

Fig. 2. Half-bridge surrogate network topology.
FIGURE 5 HALF BRIDGE NETWORK TOPOLGY

IGBT/diode in a single SM. As a result, no matter how many SMs are in a valve, there are only two or four switching elements for the half or full bridge in the surrogate network.

III. REAL-TIME SIMULATION CONFIGURATION

FOR MMC-HVDC SYSTEM The proposed surrogate network for the MMC stopcock model is enforced in both processor and FPGA tackle. The real- time MMC-HVDC simulation system, as illustrated in Fig. 4, includes the power system RTDS, FPGA- grounded MMC stopcock model, and MMC physical controller. Numerous testing and exploration conditioning, similar as MMC system operation, fault analysis, and control strategy verification, can be carried out using this configuration. The power system RTDS is processor- grounded, distributed, resemblant processing tackle armature. It's extensively used for real- time simulation of electric power system and hardware in-the-circle testing of control and protection bias. It runs on a small time- step of ~2.5 us for bluffing the MMC-HVDC systems. A Bergeron traveling- surge transmission line (t- line) model having a traveling- time of1/2 small time- step is used to insulate the MMC stopcock model on the FPGA from the rest of VSC-HVDC network on the RTDS. The main advantage of using this transmission line is that the switching effect being on the MMC stopcock model has no impact on the conductance matrix of the VSC-HVDC system. This avoids the need for reinverting or putrefying the system conductance matrix. Also, the configuration of the interface transmission line permits the MMC stopcock model to be connected between any two bumps in the small time- step network. This provides demanded inflexibility in connecting the MMC stopcock model into the small time- step network. The MMC side of the interface transmission t- line is also shown inFig. 3. Due to the successional prosecution nature of the processor, veritably limited number of SMs can be dissembled in a processor in real time. For illustration, only 40 full- ground SMs or 50 half- ground SMs can be modeled on a PowerPC MPC7448 processor running at1.7 GHz. Also, a large number of I/ O cards are needed to affiliate between the processor- grounded MMC stopcock model and physical regulator. In this paper, only FPGA- grounded MMC-HVDC simulation tackle isdescribed.The FPGA- grounded MMC stopcock model is enforced on a Xilinx ML-605 FPGA board. The Virtex 6 FPGA on the board features 240k sense cells, 14-kb block RAM, 768 DSP48 blocks, and 24-Gb transceivers GTX furnishing up to6.6-Gb/ s data rate. It's plant that three separate stopcock models, each containing 512 SMs can be modeled on a single FPGA.Fig. 5 shows the block illustration of the FPGA- grounded MMC stopcock model. The communication interface module is used to establish the communication with the RTDS and external regulator. In addition, inFig. 4, one fiber string is connected to the RTDS and two fiber lines per stopcock are connected to the external regulator. The data communicated between the FPGA- grounded MMC stopcock model and MMC physical regulator are the capacitor voltages Vc shoot to the regulator and blasting control words transferred back to the stopcock. Using a named 2 Gb/ s line rate, four small time way (~ 10 us) is sufficient to transmit 512 SMs capacitor voltages per stopcock to the MMC regulator. One small time step (~2.5 us) is enough to bring back the 512 blasting control words with each blasting control word conforming of eight double bits. The Sunup communication protocol is used for the communication between FPGA- grounded MMC stopcock and external regulator. The complete original network shown inFig. 3 is answered in the Dommel network solver shown inFig. 5. This includes the computation of the branch voltages and streamlined history current/ voltages Ihtl, Vhrl, Vh1, and Vh2 for the corresponding section (t-line, reactor, blocked SM, and deblocked SM).

IV. CONCLUSION

The main ideal of this paper was to dissect the current technologies used for transmitting power, fastening on HVdc systems. The enabling objects were to make a simulation model of an HVdc system between to power grids, to apply a sensorless regulator for grid synchronization of an MMC-grounded HVdc terminal, and to dissect the impact of a high-voltage, presto- switching IGBT's on an MMC- grounded terminal. This paper has fulfilled the following

- A theoretical background was given of HVdc technologies, fastening on MMCs. From this background it was concluded that the MMC has several advantages over other HVdc-VSC topologies so it's a feasible volition for HVdc-VSC links, especially when trying to connect to weak ac grids.
- A first order transfer function to model the MMC factory was presented. Once a PI regulator is added to control the factory, it becomes a alternate order transfer function that facilitates the design the current regulator of the MMC. The process was shown and validated with simulations.

There's an adding demand for real- time simulation of MMC- grounded HVDC in ultramodern power systems. Therefore, the effective modeling of MMC stopcock and important simulator tackle enabling simulation of hundreds of SMs in a many forever's are largely desirable. This paper describes an effective MMC modeling approach and presents the FPGA- grounded MMC simulation tackle. With devoted resembling tackle armature and deep pipelined computational machine, three independent faucets with over to 1536 SMs are suitable to be dissembled in a single FPGA in a2.5 μs time- step. The presented fashion and simulation tackle are successfully applied to test the control system for the world's first three-terminal MMC-HVDC system in China. Meanwhile, a variety of trials have been done using the real-time simulator before the real system is connected to the real grid. The flash results from the real-time simulation show good agreement with those from on- point testing and PSCAD/ EMTDC off- line simulation. MMC followed a analogous process to the one followed for a two- position inverter. This facilitates the process of erecting a simulation model for individualities formerly familiar with a three-phase two- position inverter control. A prefilter was added to reference command of the regulator to insure the named bandwidth was achieved. Without a prefilter, the system bandwidth is further than twice the named design target.

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