

SIMULATION ANALYSIS OF HIGH STEP UP QUASI-Z SOURCE DC-DC CONVERTER

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Abstract: - In this paper a high step-up quasi-Z Source (QZS) dc-dc converter is proposed. This converter uses a hybrid switched-capacitors switched-inductor method in order to achieve high voltage gains. The proposed converter have resolved the voltage gain limitation of the basic QZS dc-dc converter while keeping its main advantages, such as continuous input current and low voltage stress on capacitors. Compared to the basic converter, the duty cycle is not limited, and the voltage stress on the diodes and switch is not increased. In addition to these features, the proposed converter has a flexible structure, and extra stages could be added to it in order to achieve even higher voltage gains without increasing the voltage stress on devices or limiting the duty cycle. The operation principle of the converter and related relationships and waveforms are presented in the paper. Also, a comprehensive comparison between the proposed and other QZS based dc-dc converters is provided which confirms the superiority of the proposed converter. Simulations are done in Matlab Simulink in order to investigate the maximum power point tracking (MPPT) capability of the converter. In addition, the valid performance and practicality of the converter are studied through the results Simulink.

Keywords :- QZS, DC-DC, Converter, MPPT, etc.

1. INTRODUCTION

Sun is the limitless sources that people can profit by it. But the solar panel process has taken some money. To obtain electricity, this method is very expensive and the efficiency is very low such as 19 % - 24 %. But by using some devices that has called MPPT (maximum power point tracking), the efficiency and the gain can be increased in voltage level. Maximum power point tracker is the booster that boost the output of photovoltaic array under the control strategies. MPPT can increase the solar panel dc voltage using dc to dc converter topologies. Using this way, lower voltage value can be increased to desired voltage level and can be converted to AC. In terms of structures of the ordinary or common dc to dc topologies have boundaries to handle perfect efficiency and high gain in renewable energy sources or other any systems. A novel unique topology that has an original impedance link to combine the source and main circuit. This was a z source dc to dc converter. First z-source topology has presented by Fang Zheng Peng in 2003 and some papers have been published by researchers since 2003. This thesis will explain the z-source dc to dc converter topology that has a unique efficiency, minimal cost and perfect stability. With unique structure, inrush currents and harmonic distortion have been taken down to minimal value. Also, 300 Watt system will be designed and simulated in following sections. Also filter inductor design

will be explained in following sections. Not only in MPPT but the z-source topology can be used in all converter applications (ac-ac, dc-ac, ac-dc, and dc-dc). Z-source dc to dc topology shown in Fig-1.

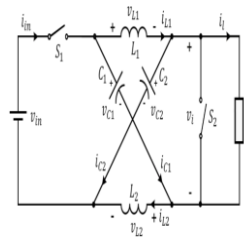


Figure 1: Z-source dc to dc converter circuit

It has z shaped two inductors and two capacitors that couple the system to the load and source. The value of capacitors and the value of inductances are equal. Pulse with modulation (PWM) technique will be used to switch the switches. The output voltage can be set to any higher value depend to the duty cycle of the switch. Also depend to the duty cycle, output can be adapted to buck or boost. This feature makes the z-source topology takes one step ahead of traditional topologies (Peng, 2003). Every chosen parameter is very important for the efficiency, stability and cost. Therefore, the system design and calculations must be done very carefully and simulation tests are necessary. The detailed explanations will be presented following chapters. Every step will be described one by one and also simulation test will be explained using MATLAB Simulink. Moreover, advantages will be explained following chapters. All operations have been operated and explained with CCM (continuous conduction mode). Considering the above-mentioned drawbacks, using transformer or coupled inductors is not a proper method to improve the voltage gain of QZS network. Another method which has been presented in this paper is cascading several modules of QZS network to increase the total voltage gain. But, in this method, the number of components is notably increased. This results in high power loss, low efficiency, high possibility of failure, and low reliability of the whole system.

QUASI Z-SOURCE DC-DC CONVERTER

The z-source topology is the converter that converts voltage level to upper or lower levels. It means that is dc to dc boost converter or buck converter. Z shaped inductors and capacitors can couple the system. When it does that, it uses unique inductor-capacitor network that has an impedance. Thus, the harmonic distortion and inrush current have been reduced to minimal value. Z-source inductors and capacitor have been chosen same value. So, they can be used symmetrical. The inductor voltages and capacitor voltages will

be equalized due to symmetrical properties. So, the voltages will be following equation.
 $V_{L1} = V_{L2} = V_L$ and $V_{C1} = V_{C2} = V_C$
 Inductor-capacitor (LC) filter used to take down output voltage ripple. Z-source dc to dc topology shown in Figure-2.

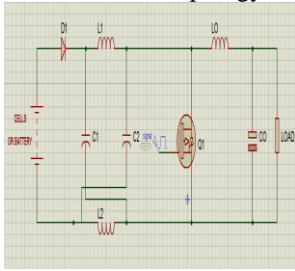


Figure 2: Schematics design of z-source dc to dc converter

Description of Application

Working principle of the circuit will be explained in 2 working steps. For step 1, D1 is in conduction and Q1 is turned off state. Supply voltage (V_s) (cells or battery) supply energy to the z-source capacitors. Simultaneously, z-source inductors transfer their energy to the load.
 Step 1 interval: $(1-d)T$.
 d ; duty cycle
 T ; switching cycle, period.

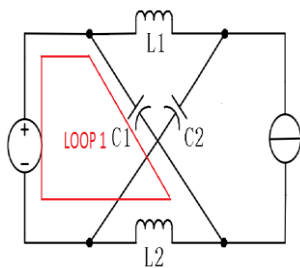


Figure 3: Z-source LOOP 1 switch turn OFF state

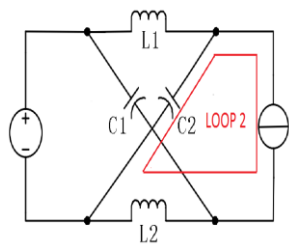


Figure 4: Z-source LOOP 2 switch turn OFF state

In this step, z-source capacitor and output voltage can be written as Figure 3 and Figure 4;
 LOOP 1; $V_c = V_s - V_L$

$$\dots\dots\dots (3.1)$$

LOOP 2; $V_o = V_c - V_L = V_s - 2V_L$

$$\dots\dots\dots (3.2)$$

For step 2, D1 is in non conduction mode and Q1 is ON. Inductor starts to store energy for release it towards to the load.
 Step 2 interval; dT

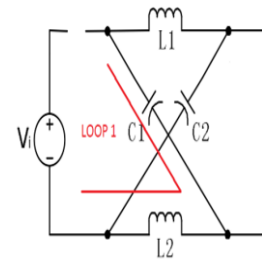


Figure 5: Z-source LOOP 1 turn ON state

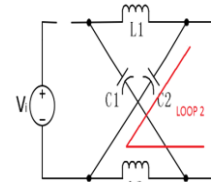


Figure 6: Z-source LOOP 2 turn ON state

As seen on schematics, the path will be;
 LOOP 1; $V_c = V_L$

$$\dots\dots\dots (3.3)$$

LOOP 2; $V_o = V_c - V_L = V_L - V_L = 0$

$$\dots\dots\dots (3.4)$$

The step 2 can also be shown in Figure 3.6.

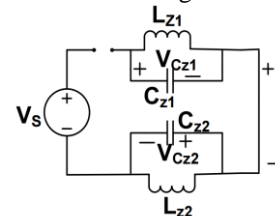


Figure 7: Equivalent of step 2

The voltage on inductor in step 2 is;
 $V_L = L \times (di/dt)$, in step 2 inductor voltage is equal to the capacitor voltage V_c . So the equation will be;
 $V_L = V_c = L \times (di/dt)$.

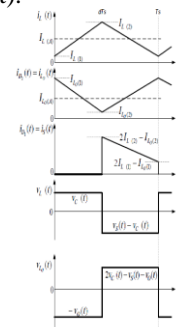


Figure 8: Waveforms of several parameters

Design of the Converter

The important parameters of design a z-source converter are the passive components, duty cycle and switching frequency. Low frequency means that the passive components will be increased, and physical dimension of the circuit will increase. On the other hand, to keep low the sizes of passive components, also will decrease the physical dimension of circuit. Therefore, the frequency should be high, however, the losses will be increased and efficiency problem will be emerged. The frequency has been chosen 50 kHz for the following example

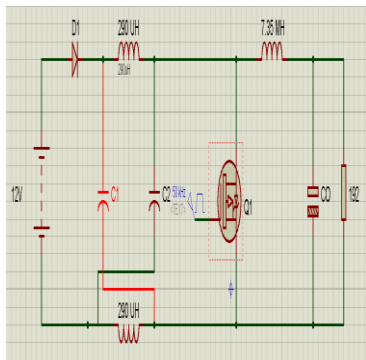


Figure 9: ISIS proteus schematic z-source circuit

In the example circuit, 12 V input voltage, 200 V output voltage and 208 W output power will be provided.

The calculations will be depended to these parameters.

- $V_s = V_{in} = 12 \text{ V}$
- $V_o = 200 \text{ V}$
- $P_o = 208 \text{ W}$
- $R_L = 192 \Omega$
- $f = 50 \text{ kHz}$
- $I_{Load} = V / R = 200 / 192 = 1.04 \text{ A}$

To find duty cycle, equation 3.14 will be used

$$D = (V_o - V_s) / (2V_o - V_s) = (200 - 12) / (2 \times 200 - 12)$$

$$d = 0.4845 = 0.49$$

To find inductor value of z source network, inductor current ripple of z-source network should be calculated. To calculate inductor current ripple of z-source network, inductor current of z-source network should be calculated.

The following equation for I_L ;

$$I_L = ((d-1)^2 \times V_s) / (R_L \times (1-2D)^2)$$

$$I_L = ((0.49-1)^2 \times 12) / (192 \times (1-2 \times 0.49)^2)$$

$$I_L = 3.12 / 0.076$$

$I_L = 40.625 \text{ A}$ is the z-source network inductor current.
The z-source inductor ripple has been assigned to 20%.
Then,
 $i_L = 8.12 \text{ A}$ for 20%.

To find z-source inductor value;

$$L_z = (V_o \times d \times T) / \Delta i_L$$

$$L_z = (200 \times 0.49 \times 0.00002) / 8.12$$

$$L_z = 241 \times 10^{-6} \text{ H}$$

To find output inductor value of the circuit, output inductor current ripple of the circuit should be calculated.

To calculate output inductor current ripple of the circuit, output inductor current of the circuit should be calculated.

The following equation for I_{Lo} ;

$$I_{Lo} = ((1-d) \times V_s) / (R_L \times (1-2D))$$

$$I_{Lo} = ((1-0.49) \times 12) / (192 \times (1-2 \times 0.49))$$

$$I_{Lo} = 6.12 / 3.84$$

The final result of the output inductor current will be;
 $I_{Lo} = 1.59 \text{ A}$

The output inductor current ripple has been assigned to 20%.
The 20% of the output inductor current ripple is 0.32A

$$\Delta i_{Lo} = V_o \times dT / L_o$$

$$L_o = V_o \times dT \Delta i / L_o$$

$$L_o = 200 \times 0.49 \times 0.00002 / 0.32$$

$L_o = 6.125 \text{ mH}$ is the output inductor value.

2. PROPOSED WORK

Principles of Operation

Fig. 10 shows the proposed high step-up qZS-based converter. As observed, a synchronous switch S_2 is employed in place of the diode existing in the qZS network. Also, a voltage-extending cell consisting of an inductor L_2 coupled to the inductor L_1 (one of the inductors of the qZS network), a diode Do_2 , and a capacitor Co_2 , is included to increase overall voltage gain. The coupled inductor is modelled by a magnetizing inductance L_m , a leakage inductance L_{lk} referred to the secondary side, and an ideal transformer. C_{s1} and C_{s2} are the snubber capacitors across the power switches S_1 and S_2 , respectively.

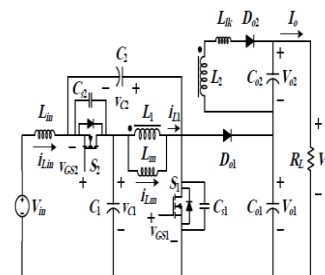


Fig. 10 Proposed high step-up qZS converter

The output capacitors Co_1 and Co_2 are assumed to be large enough such that their voltage ripples over a switching cycle can be ignored. On the other hand, C_1 and C_2 have voltages with small ripples compared to their average values. Similar to a converter with an active clamp circuit, S_1 and S_2 are switched in complementary with short dead time between turn-off of one switch and turn-on of another. The input inductor L_{in} is large enough to operate in continuous conduction mode over the entire range of load variations. While, the magnetizing inductance L_m is small in value such that its current direction varies between positive and negative within one switching cycle.

The proposed converter has seven operating modes within one switching cycle. Equivalent circuit of the proposed converter within each mode and its corresponding theoretical waveforms are shown in Fig. 11 and Fig. 12, respectively. Prior to Mode 1, it is assumed that S_1 is OFF, S_2 is ON, and the output diodes Do_1 and Do_2 are both reverse biased. Also, magnitude of i_{Lm} is linearly increasing in negative direction. Since the magnitude of i_{Lm} is greater than i_{Lin} , the current is flowing through S_2 in positive direction.

Mode 1 [t_0, t_1]: At t_0 , the power switch S_2 is turned OFF. Existence of the snubber capacitors limits the variation rate of the voltage across S_2 , so that it turns OFF under ZVS

condition. The current difference between the magnitudes of iLm and $iLin$ discharges $Cs1$ and charges $Cs2$. When the voltage across $Cs1$ reaches zero, body diode of $S1$ conducts and this mode ends.

Mode 2 [$t1, t2$]: Conduction of the body diode causes the voltage across $S2$ to be clamped to $VC1+VC2$. Also, $vC1$ is applied to Lm and magnitude of its current starts decreasing. Meanwhile, a resonance between the capacitor $C1$ referred to the secondary-side of the coupled inductor and the leakage inductance Llk occurs which makes $Do2$ start conducting under ZVZCS condition. While its body diode is conducting, $S1$ can be turned ON under ZVS condition at any moment. The magnitude of iLm still decreases until it becomes zero and then the current rises in positive direction. The sum of $iLin$, iLm , and the resonant current referred to the primary side flows through $S1$. The resonance of $C1$ and Llk continues until the resonant current becomes zero and $Do2$ turns OFF under ZVZCS condition.

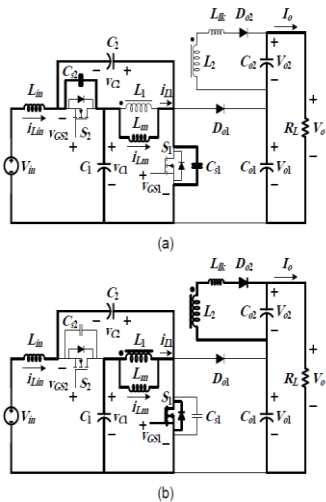


Fig. 11. Equivalent circuit of the proposed converter within each mode. (a) Modes 1 and 4. (b) Mode 2.

Mode 3 [$t2, t3$]: After the resonant current becomes zero, $S1$ conducts the sum of $iLin$ and iLm . Also, voltage across $Do2$ remains near zero, since the voltage difference between $n vC1$ and $Vo2$ is small. This mode continues until $S1$ is turned OFF.

Mode 4 [$t3, t4$]: At $t3$, $S1$ turns OFF under ZVS condition due to existence of the snubber capacitors. The sum of $iLin$ and iLm charges $Cs1$ and discharges $Cs2$. When the voltage across $Cs2$ reaches zero, body diode of $S2$ conducts and this mode ends.

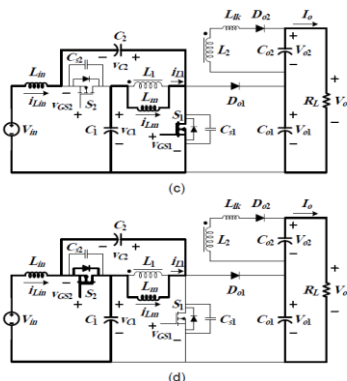


Fig. 12 Equivalent circuit of the proposed converter within each mode. (c)

Mode 3. (d) Modes 5 and 7

Mode 5 [$t4, t5$]: After conduction of the body diode, voltage across $S1$ is clamped to $VC1+VC2$. Since the sum of $vC1$ and $vC2$ is initially smaller than $Vo1$, the output diode $Do1$ remains reverse biased. However, its voltage is near zero regarding the small voltage difference between $VC1+VC2$ and $Vo1$. On the other hand, $vC2$ is inversely applied to Lm and its current starts decreasing. While its body diode is conducting, $S2$ is turned ON under ZVS condition. Therefore, the current is forced to pass through the MOSFET instead of its body diode. This reduces the switch conduction loss, since MOSFET exhibits lower voltage drop compared with its body diode. During this mode, $C1$ and $C2$ are charging and their voltages are increasing.

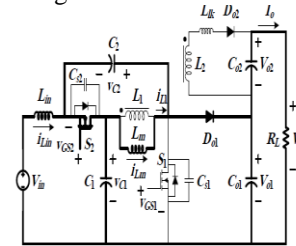


Fig.13 Equivalent circuit of the proposed converter within each mode. (e) Mode 6

Mode 6 [$t5, t6$]: Once the sum of $vC1$ and $vC2$ reaches $Vo1$, the output diode $Do1$ starts conducting under ZVZCS condition. Therefore, a part of $iLin$ and iLm is delivered to $Co1$. The current iLm still decreases until it reaches zero and then becomes negative.

When the magnitude of iLm in negative direction becomes larger than $iLin$, direction of the current flowing through $S2$ reverses. It is necessary that the current of $S2$ become positive before it turns OFF to ensure the snubber capacitors are charged/discharged in the next cycle.

This mode ends when the current of $Do1$ becomes zero and the diode turns OFF under ZVZCS condition.

Mode 7 [$t6, t7$]: $S2$ conducts the current difference between the magnitudes of iLm and $iLin$. This mode continues until $S2$ is turned OFF again at the beginning of the next cycle.

3. SIMULATION AND RESULTS

Matlab Simulation High Step-up DC to DC Converter

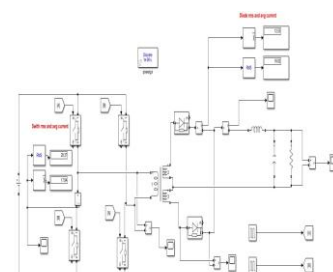


Fig 14- Matlab Simulation of Isolated DC to DC Converter

- In this Matlab Simulation the proposed converter utilizes a qZS inverter, a high-frequency step-up isolated transformer, a VDR, and a load.

- It consists of one inductor, three capacitors, diodes, four power switches, and one step-up high-frequency transformer.
- Compared to the qZS based isolated DC-DC converter, the proposed converter has one more diode and one less LC pair.
- Because the input voltage is directly connected to the inductor, the source current in the proposed converter is continuous.

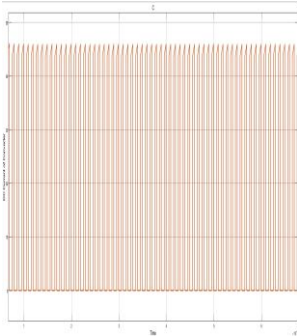


Fig 15- Simulation Results of DC Converter Output Current

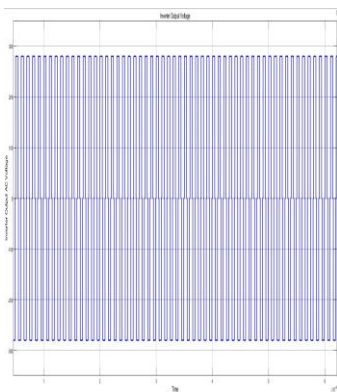


Fig 16- Simulation Results of Inverter Output AC Voltage

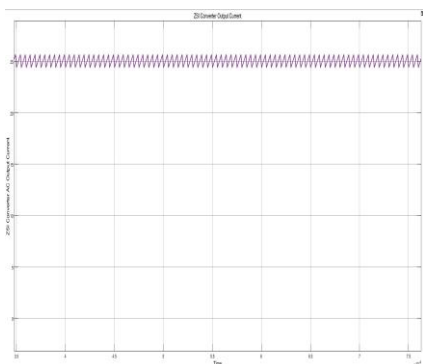


Fig 17- Simulation Results of ZSC DC Output Current

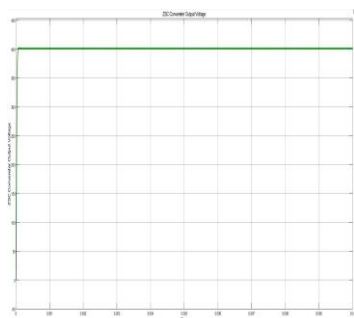


Fig 18- Simulation Results of ZSC DC Output Voltage

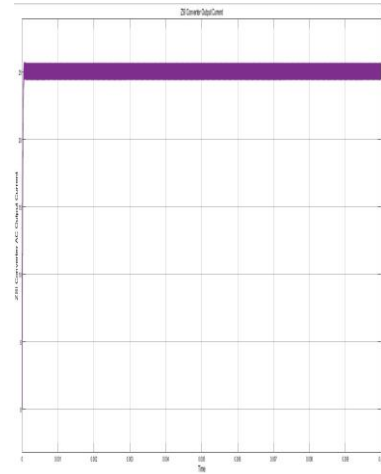


Fig 19- Simulation Results of ZSC DC Output Current

Matlab Simulation High Gain Isolated DC to DC Converter

- Compared to the quasi-Z-source-based isolated DC-DC converter, the proposed converter uses fewer passive components.
- The operating principles, analysis, parameter design guideline, and comparison with the quasi-Z-source-based isolated DC-DC converter are presented.
- The proposed converter is applicable for distributed power generation applications where a varying low dc input voltage is converted to a high stabilized dc output voltage with a galvanic separation requirement.

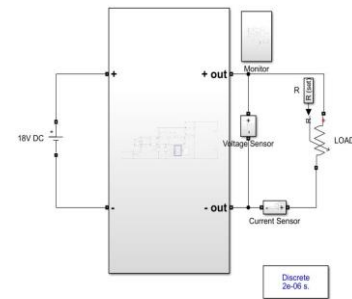


Fig 20- Matlab Simulation of High Gain DC to DC Boost Converter

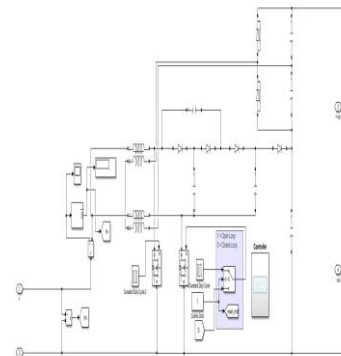


Fig 21- Isolated DC to DC Converter Subsystem

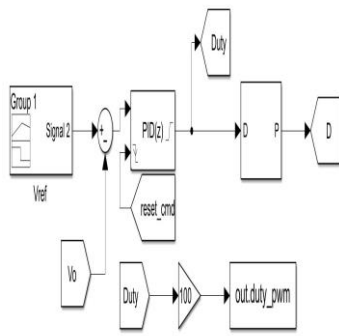


Fig 22- Controller subsystem for closed loop operation of proposed system

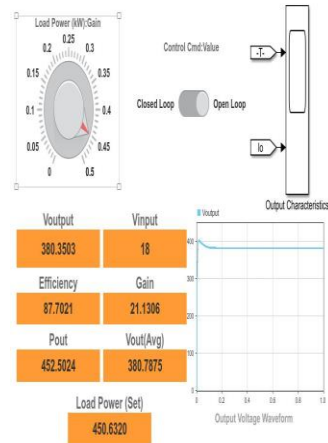


Fig 23- Simulation Results of Proposed System with Open Loop Operation

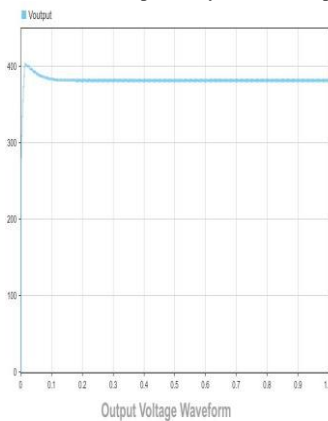


Fig 24- Simulation Waveform of Output Voltage for Proposed Converter with Open Loop Controlling

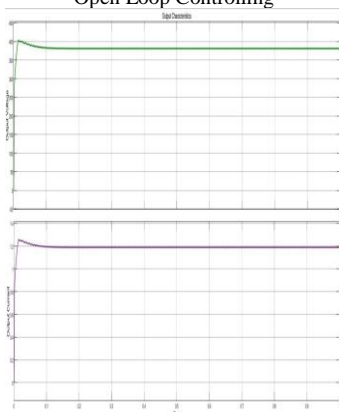


Fig 25- Simulation Results of Output Voltage and Current for Proposed Converter with Open Loop Controlling

Voutput	Vinput
380.3503	18
Efficiency	Gain
87.7021	21.1306
Pout	Vout(Avg)
452.5024	380.7875
Load Power (Set)	
450.6320	

Fig 26- Simulation Reading of Different Parameters with Open Loop Controlling

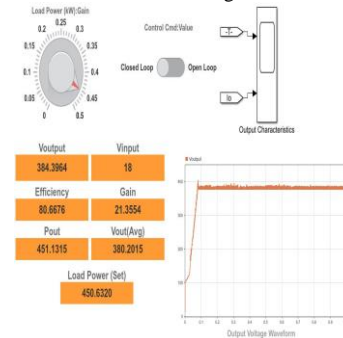


Fig 27- Simulation Reading of Different Parameters with Closed Loop Controlling

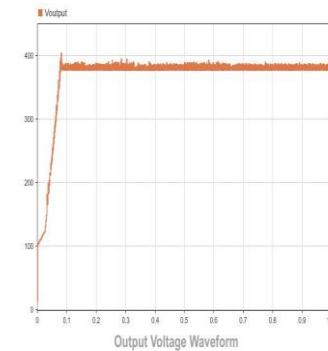


Fig 28- Simulation Waveform of Output Voltage for Proposed Converter with Closed Loop Controlling

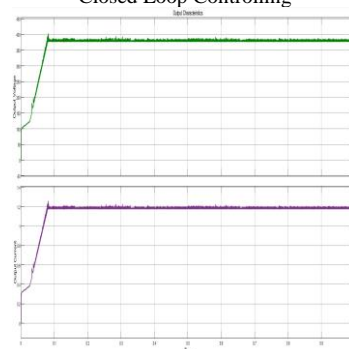


Fig 29- Simulation Results of Output Voltage and Current for Proposed Converter with Closed Loop Controlling

V. CONCLUSION

In this paper a high step-up quasi-Z Source (QZS) dc-dc converter is proposed. This converter uses a hybrid switched-capacitors switched-inductor method in order to achieve high voltage gains. The proposed converter have resolved the voltage gain limitation of the basic QZS dc-dc converter while keeping its main advantages, such as continuous input current and low voltage stress on capacitors. Compared to the basic converter, the duty cycle is not limited, and the voltage stress on the diodes and switch is not increased. In addition to these

features, the proposed converter has a flexible structure, and extra stages could be added to it in order to achieve even higher voltage gains without increasing the voltage stress on devices or limiting the duty cycle. A novel Z-source dc-dc converter was proposed in this paper. By PWM duty ratio control, it can buck or boost the input voltage. It can reduce cost and improve reliability. Its source can be voltage-source or current-source. The operating principles, analysis, parameter design guideline, and comparison to the quasi-Z-source-based isolated DC-DC converter are presented.

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