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STUDY OF SHORT CIRCUIT FAULT DETECTION IN CASCADE H-BRIDGE MULTILEVEL INVERTER

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Abstract: - This work propose Cascaded H-bridge (CHB) 7level inverter topology. Various switching frequency based PWM techniques such as Selective Harmonic Elimination PWM (SHEPWM), Optimized Harmonic Stepped Waveform PWM (OHSW PWM), Discrete Sine Area Equalization PWM (DSAE PWM), Sinusoidal PWM (SPWM) for constant and grid connected DC power source have been studied to mitigate the lower order harmonics Simulation has been carried out for 7-level inverter and results were presented with waveform and THD at different switches fault considering only switch short circuited type of fault conditions. Complete simulation work and results presented was carried out using MATLAB/SIMULINK software.

1. OVERVIEW

In recent years, electrical energy consumption is increasing rapidly due to the increasing demand of energy in the world. As a result of this, numerous fossil fuel sources and other resources which have great contribution in global warming due to greenhouse gases emission are largely consumed. Due to these negative impacts caused by these resources, a rapid progress in finding an alternative and renewable energy has attained a significant interest in the area of researches to eliminate the shortage of fossil fuels and reduce the global warming concern. In the last three decades, renewable energy has become a challenging field and many researchers have made renewable energy is the main focus in order to create new sustainable, natural abundance and environmental friendly energy resources. This demand of renewable energy will continue in future because the production of renewable energy sources are expected to satisfy 20% and 50% of the total energy needs in 2020 and 2050 respectively. Due to the possibility of providing energy with less dependence on the fossil fuels, various types of renewable energy resources such as solar, wind, tidal, waves, geothermal heat, hydropower, especially solar Photo Voltaic (PV) conversion have gained increased acceptance and growth in recent times. Significant advantages of PV panels include clean and reliable energy production and suitability for distributed generation.

2. TYPES OF MULTI-LEVEL INVERTERS

Many researchers have developed many multi-level inverter configurations and are several types of multi-level inverters classified based on their type of connection, components used in inverter circuit. Some of the types of multi-level inverters are:

- ❖ Diode clamped MLI or also called as Neutral clamped MLI
- ❖ Flying capacitor type MLI
- ❖ Cascade H-Bridge topology

Diode clamped inverters also known as neutral point clamped inverter topology of multi-level inverters is first developed in 1981 and later many researchers have extended the concept. As the name suggests, this type of inverters need a clamping device and make use of diodes for clamping.

a. DIODE-CLAMPED MULTILEVEL INVERTER

The used multilevel topology is the diode clamped inverter. In this topology diode is utilized as cinching gadget to brace the dc transport voltage to get ventures in the yield voltage. The Neutral Point Inverter (NPC) proposed by Nabae, Takahashi, and Akagi in 1981. It was essentially a three-level diode-clamped inverter. A three-level DCMLI consists of two pairs of switches and two diodes. Each switch pair of DCMLI works in complimentary mode. The diodes is used to provide access to mid-point voltage. In three-level inverter each phase of the inverter shares a common dc bus, which further subdivided by two capacitors into three levels. The DC bus voltage is split into three voltage levels by using two series capacitors C1 and C2. The voltage stress across each switching device is limited up to Vdc through the clamping diodes Dc1 and Dc2. The aggregate dc connect voltage is gotten a kick out of the chance to be Vdc and mid-point is directed at half of the dc interface voltage, voltage over every capacitor is Vdc/2 (Vc1=Vc2=Vdc/2). There are three different possible switching states in a three level DCMLI which apply the stair case voltage on output voltage relating to DC link capacitor voltage rate.A set of two switches is on at any given interval of time for a three-level inverter and in five-level inverter, a set of four switches are on at any given interval of time and so on. Fig-1 shows the circuit for three-level inverter DCMLI.

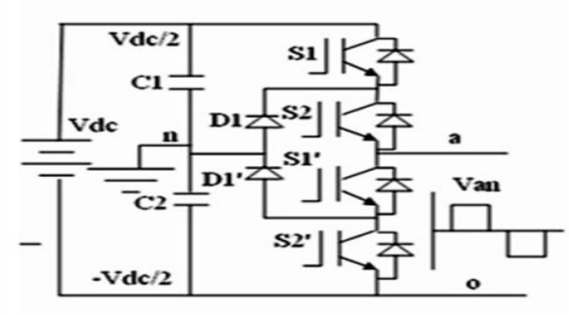

Fig 1: Three-level diode-clamped multilevel inverter

Table-1. Switching states in one leg of the three-level diode clamped inverter

Switch Status	State	Pole Voltage
S_1=ON,S_2=ON S_1'=OFF,S_2'=OFF	S=+ve	V_{ao}=Vdc/2
S_1=OFF,S_2=ON S_1'=ON,S_2'=OFF	S=0	V_{ao}=0
S_1=OFF,S_2=OFF S_1'=ON,S_2'=ON	S=-ve	V_{ao}=-Vdc/2

For N level, to make a circuit , 2(N-1) switching devices, (N-1) * (N-2) clamping diodes and (N-1) dc link capacitors are required for each leg. By expanding the quantity of voltage levels the yield voltage quality is enhanced and the voltage waveform turns out to be nearer to sinusoidal waveform becomes closer to sinusoidal waveform. In high level inverters capacitors voltage balancing becomes typical. At the point when number of level is adequately high, the quantity of diodes and the quantity of exchanging gadgets will increment and make the framework impracticable to execute.

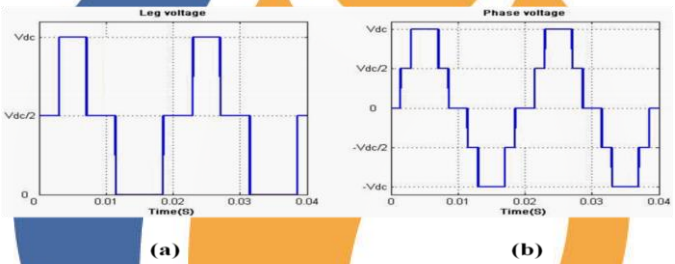

Fig: 2.Output voltage in three-level diode- clamped inverter (a) leg voltage (b) output phase voltage

2.2 FLYING CAPACITOR STRUCTURE

The capacitor clamped inverter also known as flying capacitor inverter. It was proposed by Meynardand Foch in 1992 [17]

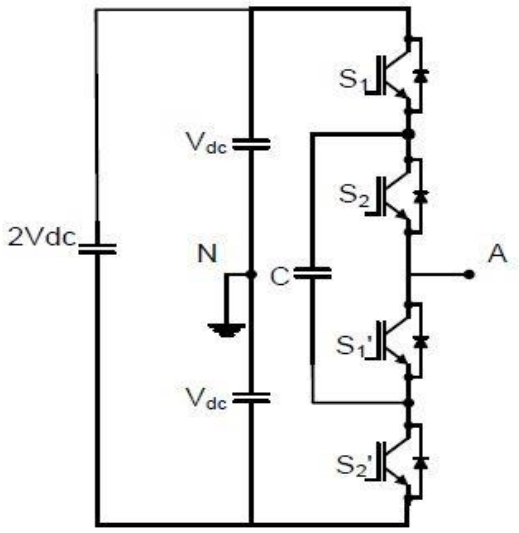

Fig.3: Three-level Capacitor-clamped multilevel inverter circuit

Its structure is similar to diode clamped inverter except that instead of using clamping diodes, capacitors are used. The flying capacitor consist of series connection of capacitor clamped switching cells. It has a ladder structure of dc side capacitors, in which the voltage of each capacitor differs from the next capacitor. The implication of voltage between two neighboring capacitor legs gives the extent of the voltage ventures in the yield waveform.

Table 2: Switching example of Flying capacitor multilevel inverter.

Output voltage $V_o=V_{an}$	Switch states			
	S_1	S_2	S_1'	S_2'
V_{dc}	1	1	0	0
0	1	0	1	0
$-V_{dc}$	0	1	0	1
	0	0	1	1

The major problem in this inverter is the requirement of a large number of storage capacitors. The voltage rating of each capacitor used is the same as that of the main power switch. For m-level converter (m - 1) x (m - 2)/2 auxiliary capacitors per phase leg in addition to (m - 1) main dc bus capacitors required[8].

With a specific end goal to make adjust the capacitor charge and release, one may utilize at least two switch mixes for center voltage levels (i.e., 3Vdc/4 in one or several fundamental cycle. The flying-capacitor multilevel converter may be used in real power conversions by proper selection of switch combinations. Nonetheless, when it includes genuine power transformations, the choice of a switch mix turns out to be extremely troublesome and the changing recurrence should be higher than the crucial recurrence.

CASCADED H-BRIDGE MULTILEVEL INVERTER

Another alternative for a multilevel inverter is the cascaded multilevel inverter or series H-bridge inverter. The series H-bridge inverter appeared in 1975[14].The CMI has been utilized in a wide range of applications. In high-power applications, it is used in shunt and series connected FACTS controllers. The CMI synthesizes its output voltage nearly sinusoidal voltage by combining several isolated voltage levels. By adding more H-bridge converters, the amount of Var can increased without redesign the power leves, and build-in redundancy against individual H-bridge converter failure can be realized.

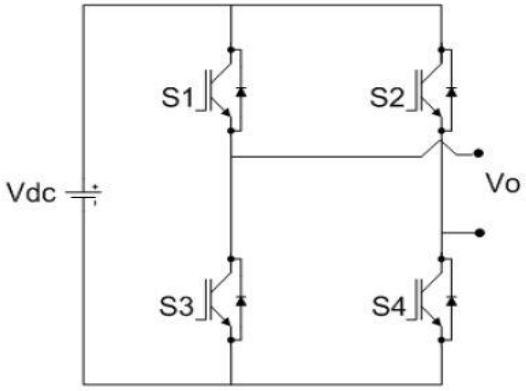

Fig 4: 3-level cascade H-Bridge Inverter

Table 3: Switching pattern of 3-level cascade H-Bridge multilevel Inverter

Output Voltage $V_o = V_{AN}$	Switch states			
	S_1	S_2	S_3	S_4
V_{dc}	1	0	0	1
0	1	1	0	0
	0	0	1	1
$-V_{dc}$	0	1	1	0

A single-phase full bridges series makes up a phase for the inverter. A three-phase CMB-MLI topology is consist of three same phase legs of the series-chain of H-bridge converters, which can generate different output voltage waveforms. This feature is impossible in other VSC structures utilizing a common DC link. As this topology consists of series power conversion cells, the voltage and power level may be easily scaled. The dc connect contribution for each full extension inverter is given independently, and this is accomplished utilizing diode rectifiers bolstered from separated optional windings of a three-stage transformer. In medium-voltage systems, phase-shifted transformers can supply the cells in order to provide high power quality.

For conversions of real power, (ac to dc and dc to ac), the cascaded-inverter needs separate dc sources. For various renewable energy sources such as fuel cell, photovoltaic, and biomass, etc. the structure of separate dc sources is well suited.

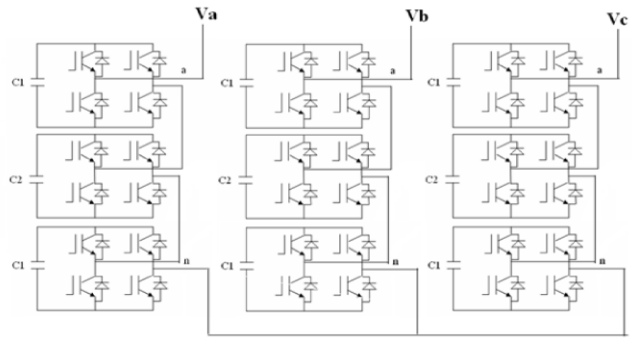

Fig. 5: Three-Phase 7-Level Cascaded Multilevel Inverter (Y-Configuration)

Association for dc sources b/n two converters in a consecutive way isn't conceivable on the grounds that a short out will be happen when converters are not exchanging synchronously.

SIMULATION MODEL

This chapter proposed seven-level Cascaded H Bridge inverter (CHB). The space vector pulse width modulation technique is applied to control the output of the anticipated inverter. The control technique has a constant switching frequency and generates reference vector of the converter using different sampling period. Also an attempt to investigate and evaluate the characteristics and operating principle of cascaded H bridge multilevel inverter. The simulation results have been carried out using MATLAB/Simulink to validate the effectiveness and feasibilities of this controlling technique

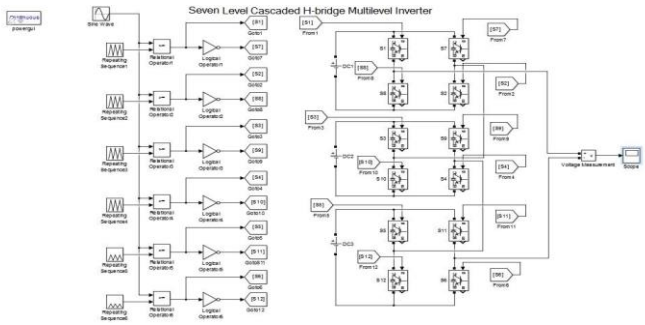

Figure 6 : Seven Level "Cascaded H-bridge Multilevel Inverter"

General circuit configuration of single phase cascaded H-bridge Nine Level Inverter is shown in Figure 4.8. Each H-bridge module has an independent DC voltage source of E. Every output terminal of H-bridge cells is connected in series. So the output voltage can be obtained by Equation (4.1) and the number of output voltage levels is obtained by Equation (4.2).

$$V_{out} = \sum_{n=1}^{k} V_n = V_1 + V_2 + V_3 + V_4 \quad 4.1$$

$$m = 2n+1 \quad 4.2$$

In Eq. (4.1), the input voltage can be Vdc, 0, or -E Vdc therefore, the output voltage is produce -4Vdc, -3Vdc, -2Vdc, -Vdc, 0, Vdc, 2Vdc, 3Vdc, 4Vdc by mixing of each output voltage.

Figure 4.9 shows the proposed PWM scheme control blocks for seven level cascaded H-bridge multilevel configuration for direct torque control scheme. Each H-bridge consists of 4 switches and one DC source, a total of 48 switches and 12 DC sources employed together to form a nine level three phase inverter.

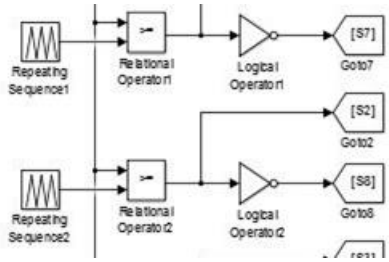

Figure 7: PWM Generator Block

RESULTS AND DISCUSSION

In our anticipated work we covered the short circuit fault (SCF). The short circuit fault (SCF) have been created in different switches and then we observe the output wave form and THD of the faults. Figure 5.1 shows the Output Waveform of Cascaded H- Bridge 7 Level Multilevel Inverter with no faults. The waveform is smooth over the time and the THD in this case is about 13.2 %

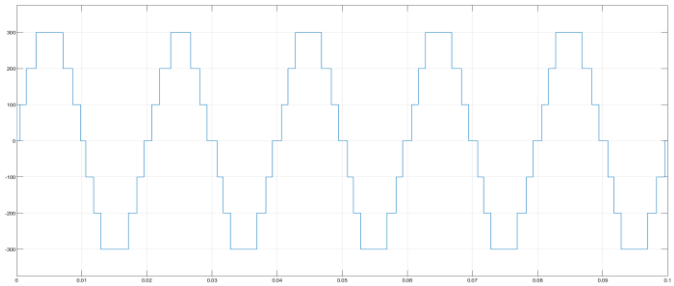

Figure 8 : Output Waveform of A"Cascaded H- Bridge 7 Level Multilevel Inverter with no faults.

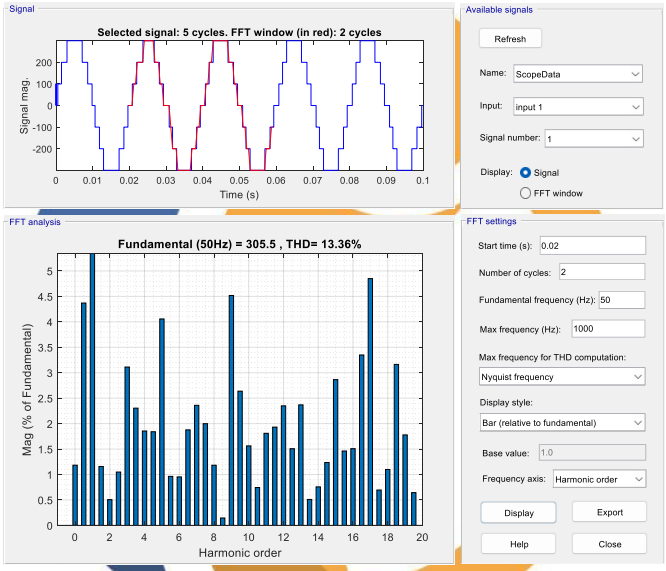

Figure 9: THD when no fault in the circuit

In preceding sections we will discuss the effect of Short Circuit Fault(SCF), the faults are created by shorting the wires in different switches.

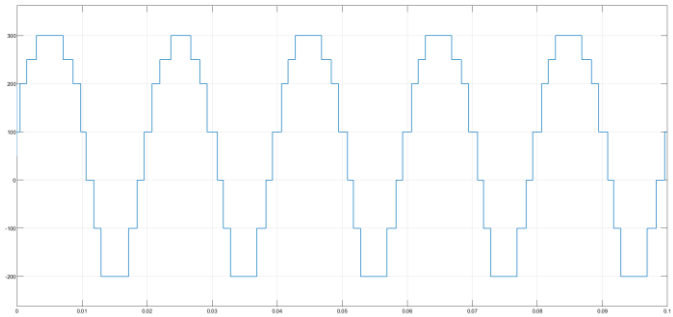

Figure 10: Wave form when Switch – S1 is short Circuited

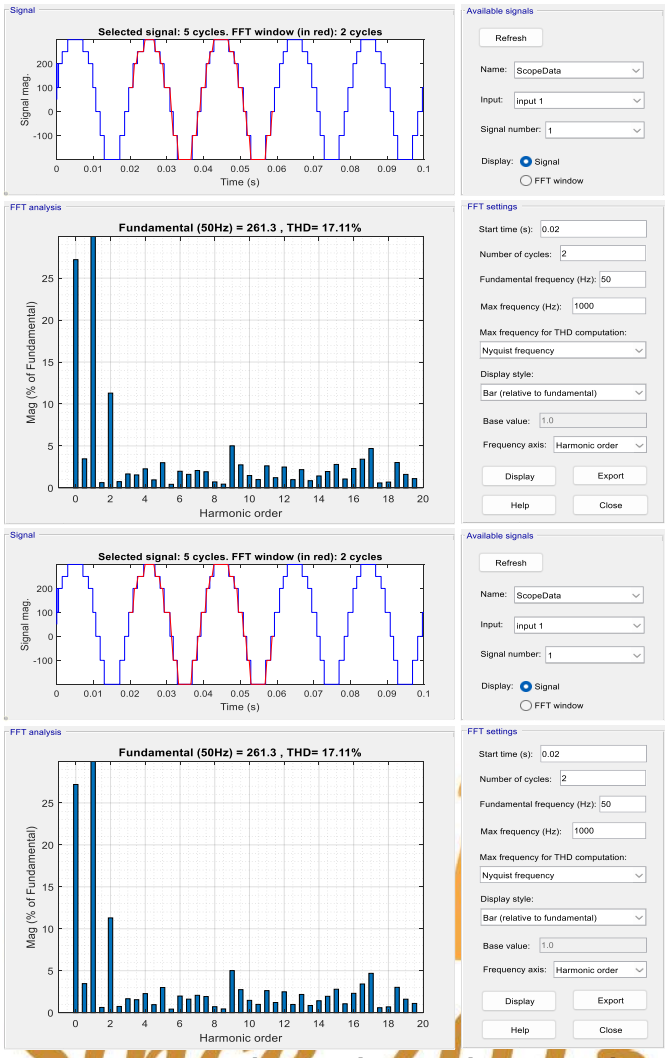

Figure 11: THD when Switch – S1 is short Circuited

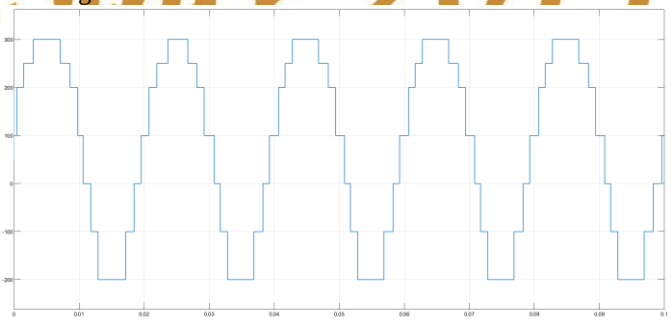

Figure 12: Wave form when Switch – S2 is short Circuited

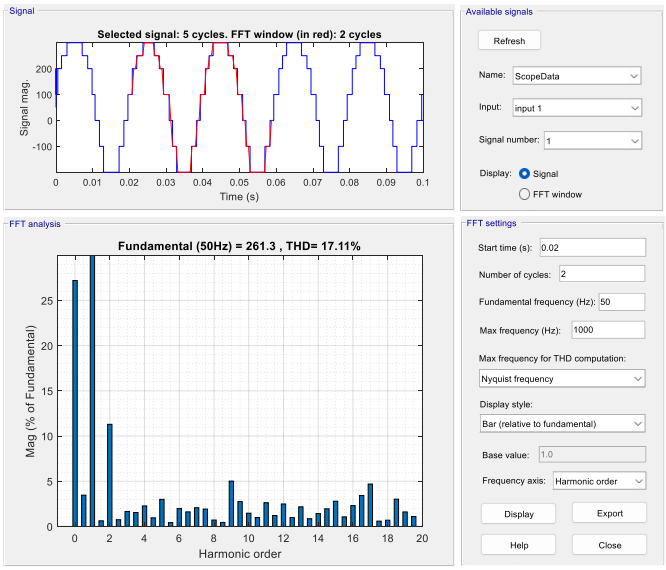

Figure 13: THD when Switch – S2 is short Circuited

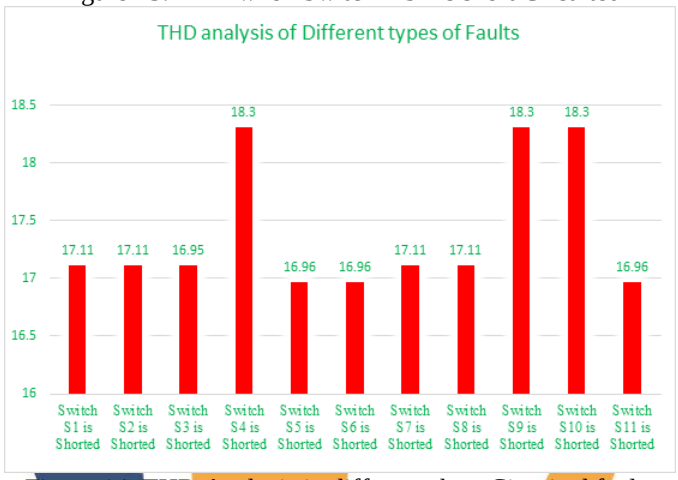

Figure 14: THD Analysis in different short Circuited faults

Figure 14 shows Total Harmonics Distortion at different shorting conditions. The THD is constant for Switch S1, S2, S3, S7 and S8 and it is 17.11 so in this case the decision for fault is tough to find. In such type of scenario we will conclude the decision by the Waveforms. The THD for faults in switch S4, S9 and S10 is also constant and it is 18.30.

Table 4: Fundamental Frequency and %THD of Phase voltages for Different Modulation technique for Conventional PWM

S. No.	Different levels of Multilevel Inverter	Phase Voltage on Fundamental Frequency	Total harmonic distortion (THD) %
1	Three	206	31.13
2	Five	210.3	18.78
3	Seven	304.7	13.20

Table 4 shows the % THD of Phase voltages for Different levels of Multilevel Inverter.

Similarly a comparison of phase voltages same inverter topologies with the THD is shown in figure 15.

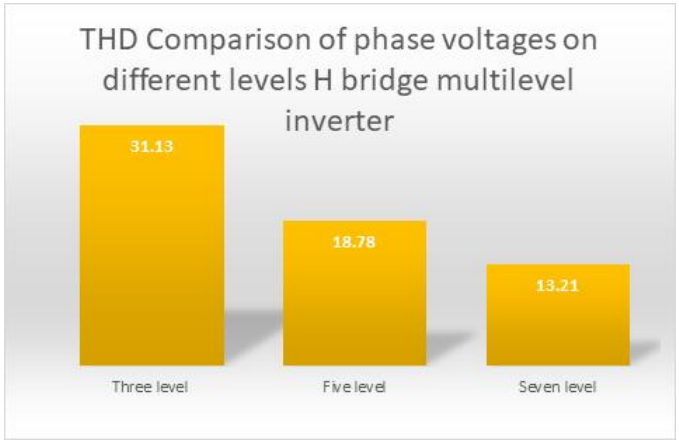

Figure 16: %THD of phase voltages for Different level technique for Conventional PWM Scheme

CONCLUSION

Cascaded H-Bridge multilevel inverters are widely used in many high power industrial applications. Any failure of power electronic switches in the multilevel inverters seriously affects the regular production in the industries. Nowadays, the development of fast and accurate fault diagnostic techniques for multilevel inverters is a serious issue. This research work focused on the development of diagnostic techniques for the identification of short switch failure of the multilevel inverters using its output voltage characteristics. Simulation results are reported on seven level cascaded H-Bridge multilevel inverter at short-switch fault conditions. Salient features are extracted from the output voltage signals at different short circuit fault conditions using FFT technique and Waveform Analysis technique. In addition, THD value of output voltage waveform are also evaluated at different Levels of H-Bridge multilevel inverter.

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