International Journal For Technological Research In Engineering
Volume 9, Issue 12, August-2022 *ISSN (Online): 2347 - 4718*

A ROBUST DESIGN OF A LOW POWER 7T SRAM CELL USING SUPPLY FEEDBACK TECHNIQUE AT 45NM FINFET TECHNOLOGY

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Abstract— Static random access memory (SRAM) is very important part of today's portable devices like camera, laptop, mobile phones. SRAM has significant impact on current electronics system. CMOS based SRAM is played vital role but leakage power, short channel effect of CMOS decreases system performance. FinFET based SRAM devices are encouraging emerging device that can be used for enhancing the performance. In this thesis , I present detail analysis of low power 7T SRAM based on FinFET at 45nm technology and comparison with 7T SRAM based on CMOS at 45nm technology. We compare various parameter like Static noise margin (read, write, hold), delays and power dissipation The design schematic has implemented on LTspice tool and simulation is carried out. We observe power dissipation is reduced, improved SNM and delay compare than 7T SRAM based on CMOS.

Keywords: FinFET based 7T SRAM, RSNM, HSNM, WSNM, Read operation, Write operation, Hold operation, leakage current, delay, CMOS based 7T SRAM.

1. INTRODUCTION

Modification has become the trend and need for electronic gadgets[1]. The Electronic appliances, gadgets, faster modes of communication, transport have advancement of technology in terms of ease in our lives and the market trend towards shifts from compact and high touch to indifferent and low touch[2]. To improve efficiency and performance of electronics devices, these circuit requires fastest memory which constitutes most part of an IC, highly reliable, low power consuming and to work at low voltage supply [3].

SRAM fulfills all the needs of because it consumes low power than DRAM and unlike DRAM, it need not refreshment as per cycle [4]. Multitude of varied approaches has been proposed both at process level and designed level to enhance efficiency and to remove the various issues like low stability, leakage and high delay etc in memories [5-6].

Standard CMOS based 7T SRAM at 45nm is mostly preferred in memory designs as it fulfills all requirements and it's read and write operation are very simple [7]. But due to short channel effect and high leakage current, its characteristics like stability, delay, noise margin affects very much.

FinFET technology has been better performing than CMOS technology at 45nm and come out as fruitful replacement for SRAM [8-10]. FinFET offer better electrostatics control over channel due to its multi-gate and non-planer structure which greatly enhance short channel effect behavior at nano -scaled level .FinFET is light body doping to minimize random dopant fluctuation .this further minimize process variation and ION and IOFF current .Due to its beneficial feature and device characteristics, FinFETs are becoming better alternate for CMOS in nano-scaled technology. Figure 1 shows 2D structure of double gate FinFET [11-14].

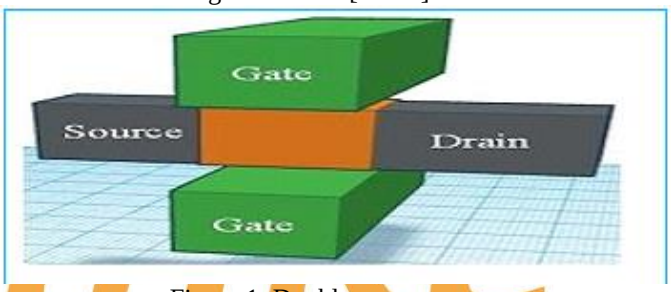

Figure 1. Double gate structure

This paper proposes a FinFET based 7T SRAM cell at 45nm technology .In this proposed design the read ,write and hold operation to improve stability. Furthermore, the supply feedback transistor has been used between data storing node and cell power supply in order to increase write operation stability of SRAM cell . With this approach the rest of paper is arranged Section II demonstrates the working of the proposed design in different modes, whereas the simulation results and discussion are given in section III. Finally, section IV concludes the proposed

II. PROPOSED DESIGN

Figure 2 depicts the proposed 7T SRAM using supply feedback concept, in which two inverter X1 and X2 and 1 DGPMOS FinFET and 2 DGNMOS FinFET are included. Q and Qb are the outputs and BL, RBL, WL are the inputs. By varying inputs, the read, write and hold operations are performed.

LTSpice model of 7T SRAM based on FinFET

This is LTspice model of 7T SRAM based on FinFET .In this model U3 is DGPMOS which provide the supply feedback and U1 and U2 are DGNMOS which is connected to BL and RBL respectively and X1 and X2 are the inverters made by FinFET. These inverters are working as a latch by varying q and Qb .to control input/output another input line i.e.

WL(word line)attached to gate terminal of FinFET U1. We provide voltage supply is 0.9v at 45nm technology. LT spice model of 7T SRAM based on FinFET is given in figure 2

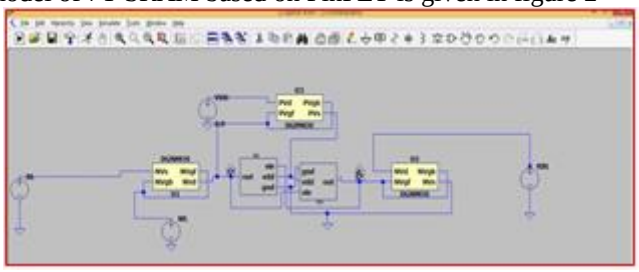

Figure 2. FinFET based 7T SRAM

3.2.1 Write Operation:

The Write operation is shown below. In write operation, The pulse input applied on BL and PWL input is applied on word line (wL) and 0V is applied on RBL .The WL switches ON the access transistor U1.The BL is driven to data level which is to be written. A conducting path between Bl and Q has been formed through access FinFET U1. During the operation write '1' at node Q (assuming 0 and 1stored at Q and Qb respectively initially) BL is driven by VDD. The given figure 3 shows the write operation.

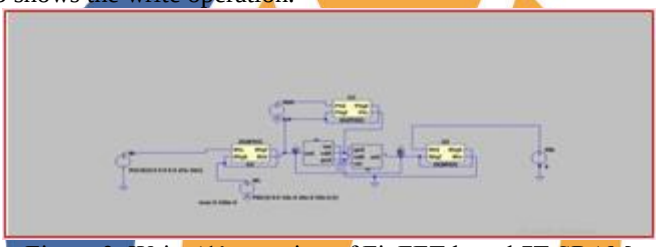

Figure 3. Write '1'operation of FinFET based 7T SRAM

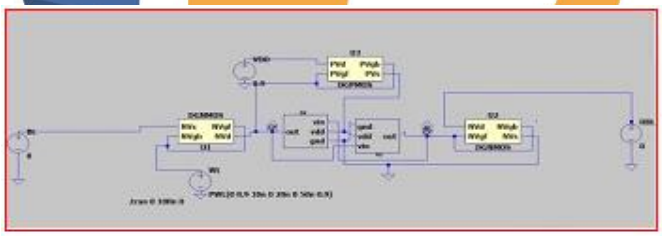

Figure 4. Write '0'operation of FinFET based 7T SRAM Read Operation:

Figure depicts the various condition of the transistors (ON or OFF) which is used in the proposed design under read operation. In this operation, WL and BL are tied to Vdd and ground respectively, while RBL is initially charged to Vdd. In read '0' mode (assuming node Q and Qb of the proposed design.

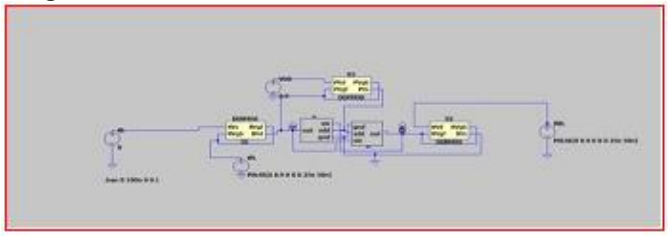

Figure 5. Read operation of FinFET based 7T SRAM

Hold Operation:

Figure 6 represents various conditions of the transistors (ON or OFF) which is used in the proposed design under hold operation. In hold operation, WL is knitted to the ground that switches OFF the transistor U1(shown by dotted in Figure is OFF, DGPMOS is ON of inverter X1 hence the node Q is retained at its desired voltage value. Due to FinFET there is no leakage current and there is no short channel effect.

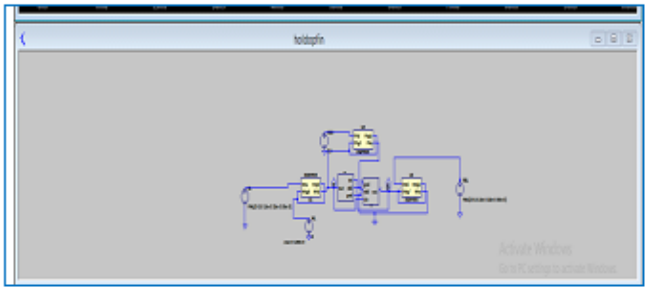

Figure 6. Hold operation of FinFET based 7T SRAM

HSNM:

The hold stability represents how the data would be retained in the cell when the SRAM cell is not performing any active operation. It is cleared by hold static noise margin (HSNM) and obtained through the butterfly curve. The butterfly graph as shown in Figure 7 for the proposed design in hold operation at 900 mV power supply. This is examined that the HSNM value of the proposed 7T is 500 mV at 900mV power supply

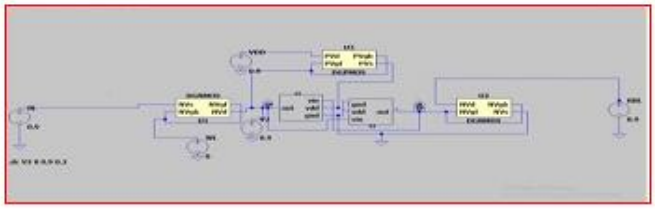

Figure 7. HSNM of FinFET based 7T SRA

RSNM:

The RSNM value represents the read stability of the SRAM cell which is examined by maximum DC noise voltage presents at the input of cross-coupled inverter pairs which unchanged the cell state without failing any data. The value of the RSNM during read operation has been achieved from the butterfly curve (plot of dc curve of back to back connected FinFET inverter) by catching the length of a side in the square that is built up in two segment of butterfly curve. The method of finding the read stability from the butterfly curve is illustrated in Figure. . It can be examined that the length of the side (in volt scale) in a square is 520 mV as shown in Figure 20. Thus this value would be the RSNM of the proposed design.

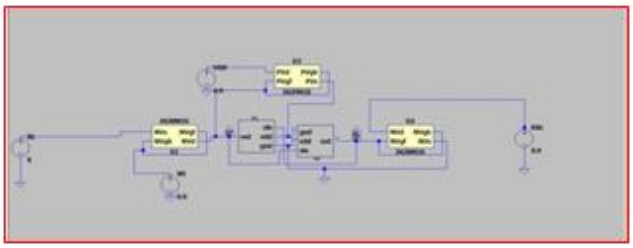

Figure 8. RSNM of FinFET based 7T SRAM

WSNM

The write ability of any SRAM cell during a write operation is described by write static noise margin (WSNM). The static noise margin in the write operation is also acquired from a butterfly graph by catching the total length of the vertical side in the square that is built up in the butterfly graph .Figure 9 represents the butterfly curve to write stability. It is indicated that the value of WSNM of proposed 7T during write operation would be 510 mV at 0.9 V cell power supply for write '0'and 590 mV for write'1' approximately.

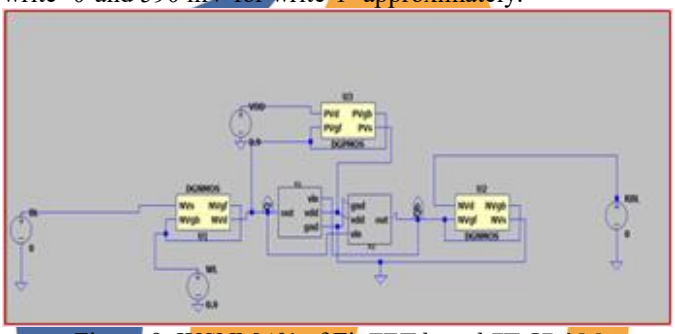

Figure 9. WSNM '0' of FinFET based 7T SRAM

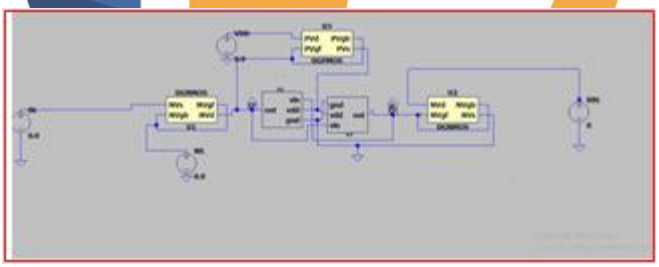

Figure 10 . WSNM '1' of FinFET based 7T SRAM

Table 1 represents the various input condition in a different mode of operation for 7T SRAM Design:

Input	Write '0'	Write '1'	Read	Hold
BL	0	1	0	1
RBL	1	1	1	0
WL	0	1	1	1

Table 1. Different mode of operation for 7T SRAM

III. RESULT AND DISCUSSION

The simulation part of the work haves been performed on LTspice tool by using 45nm Low Power FinFET based PTM technology file available on internet. The supply voltage (VDD) for this technology file is 0.9V.

The Simulation work includes the different modes and techniques and circuit parameters related to and Proposed 7T SRAM and also all the types of delays like read/write delay for logic '0' and '1', various type of Static Noise Margins(SNM) such as Hold SNM, Read SNM and Write SN

Delays and Output of Proposed 7T SRAM cell

The complete output of a proposed 7T SRAM bit cell with input applied at Bit line is shown below.

SNM of Proposed 7T SRAM cell

The Static Noise Margin (SNM) is calculated by DC Sweep method at Q node. The voltage sweep of logic '0' to '1' is applied. For Hold SNM, Word line is disabled. For, Read SNM, Word line(WL) and Reverse Bit Line (RBL) are pre charged to logic '1' and BL is set to logic '0'. For Write SNM, WL is made high and BL is set to logic'1'and RBL is logic '0' for write'1'. WL is made high and BL is set to logic'0'and RBL is logic '0' for write'0'.

The overall output of FinFET based 7T SRAM is shown below:

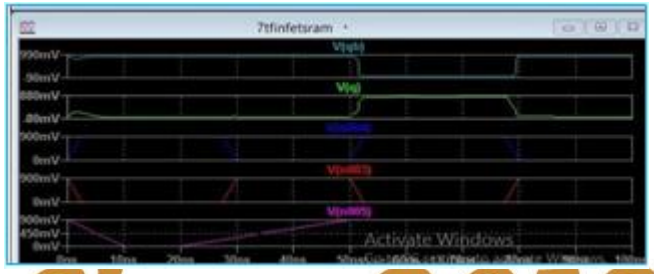

Figure 11. Overall output of Proposed 7T SRAM

Read operation initially stored logic '0' and '1' respectively) the PMOS transistor U3 goes in OFF state, DGPMOS in ON state of inverterX1 , U1 transistor in ON, and DGNMOS in OFF state of transistor X2. The transistor U2 (as gated by node Qb) would be in ON state and forms a conducting path between RBL and ground (as shown in Figure 12). RBL then starts to discharge towards the ground potential and hence the process of reading '0' has been done. Whereas for read '1' operation, the logic '1' must be stored at node Q and '0' at Qb, which tries the transistor U3 to turn OFF. As a result, it does not form the path between RBL to ground. The RBL thereby retains at its pre-charged value (Vdd)

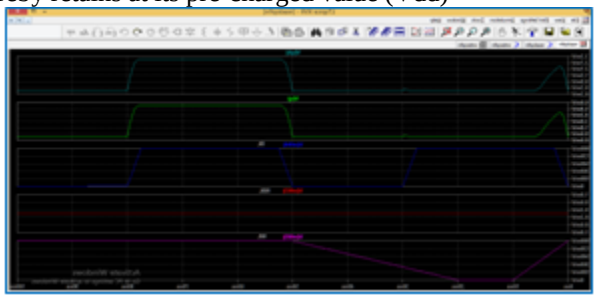

Figure 12. Simulation Result of Read Operation of Proposed 7T SRAM

Hold operation

Initially, it has been supposed that the data '0' and '1' are stored at node Q and Qb respectively (as shown in Figure 13) that turns ON the feedback transistor U3 which try to retain the same voltage at storing node Q and Qb. For the case when node Q and Qb are stored '1' and '0' respectively. The feedback transistor U3 is in cut off state DGNMOS is OFF, DGPMOS is ON of inverter X1 hence the node Q is retained at its desired voltage value. Due to FinFET there is no leakage current and there is no short channel effect.

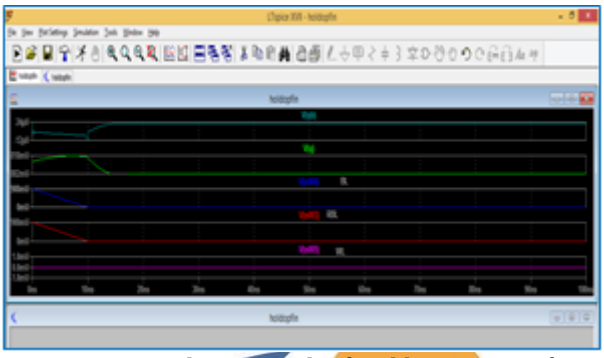

Figure 13. Simulation Result of Hold Operation of Proposed 7T SRAM

WRITE OPERATION

As WL is activated, the voltage at storing node Qb is low enough due to feedback transistor U3 which initiated the internal positive feedback and flip the data of storing nodes. The write '1' operation given in figure 1 and simulation of write '0' given in figure 15.

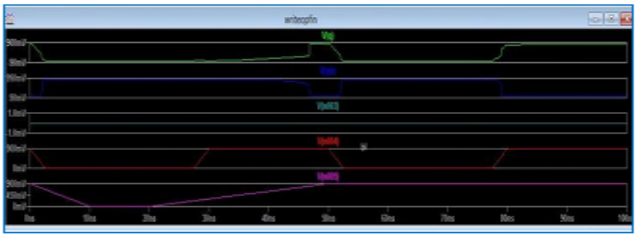

Figure 14. Simulation Result of Write '1' Operation of Proposed 7T SRAM

Similarly for writing '0' operation, the BL is driven to the ground. Initially, the feedback transistor U3 is in OFF state and provides a pull- up current which is not matched with high discharge current through transistor U1. The internal positive feedback acts and storing nodes get the desired values.

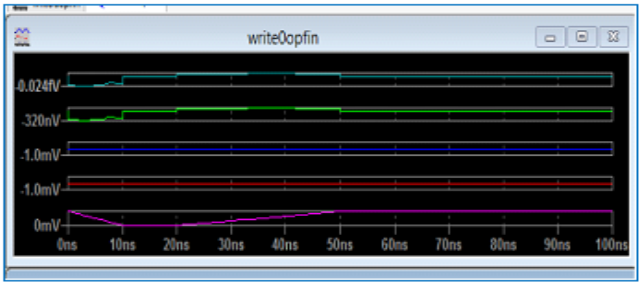

Figure 15. Simulation Result of Write '0' Operation of Proposed 7T SRAM

SNM of proposed design

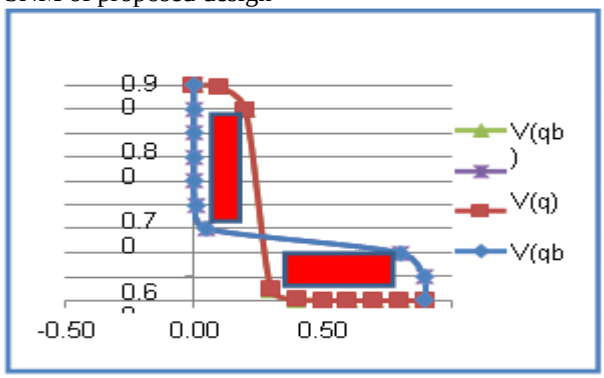

Figure 16. Simulation Result of HSNM of Proposed 7T SRAM

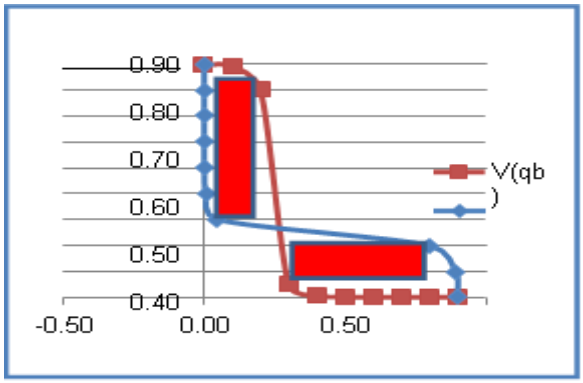

Figure 17. Simulation Result of RSNM of Proposed 7T SRAM

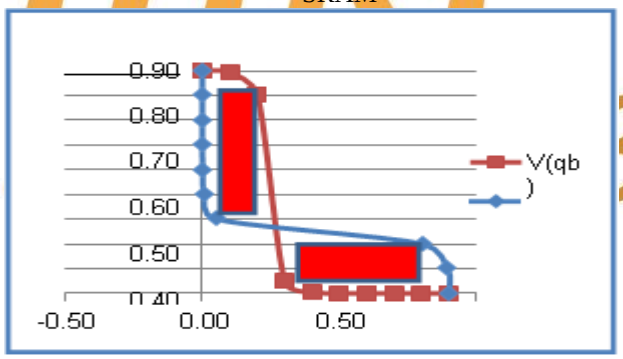

Figure 18. Simulation Result of WSNM '1'of Proposed 7T SRAM

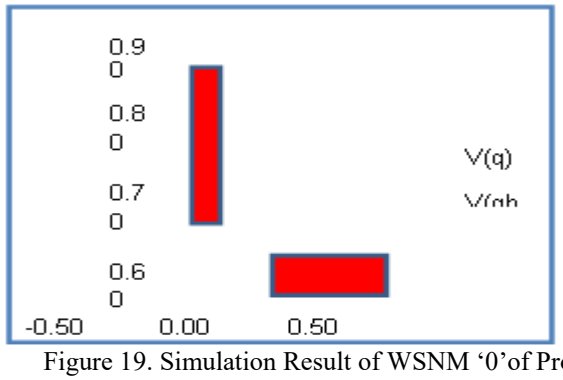

Figure 19. Simulation Result of WSNM '0'of Proposed 7TSRAM

Read and Write delay:

The read delay is a time which evaluated when read port is activated then the RBL discharge to 50% from its initial value. The read delay of the proposed design at various cell supply

voltage is shown in figure 20. The write delay evaluated as the time required to write data at storing nodes, from the time when WL reaches 50% of its final value. Figure. 21 illustrates the write delay of proposed 7T at several cell supply voltage. Below is the table of delay of various operations of proposed FinFET based 7T SRAM compared with CMOS based 7T SRAM. at 0.9 cell power supply. The slight increment in the write delay occurs due to using a supply feedback transistor in the proposed 7T.

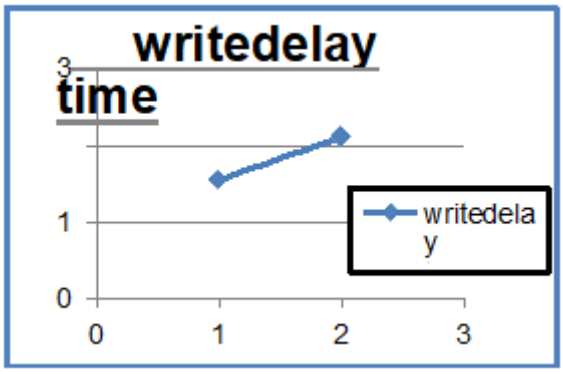

Figure 20. Write Delay of Proposed 7T SRAM

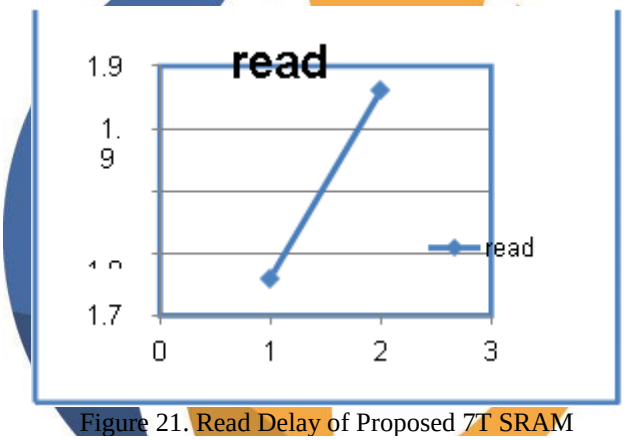

Figure 21. Read Delay of Proposed 7T SRAM

SRAM Cell	Write'1'(s)	Read'1'(s)
Standard 7T	2.62n	2.59n
Proposed 7T	1.855p	1.83p

Table 1. Comparison Table of delay of Proposed 7T SRAM and Standard 7T SRAM

The comparison of proposed 7T to other reported SRAM cell is shown in Table II. It has been observed that the proposed design have a better result as compared to 7T SRAM cell and other SRAM cell in respect to RSNM, WSNM, static power dissipation and read delay.

Parameters	6T	7T	10T	8T	8T	7T	Proposed Design
Technology (nm)	28	28	28	90	28	45	45
Supply Voltage (V)	0.9	0.9	1	1	1	0.9	0.9
RSNM (mV)	190	360	342	291	320	400	580
HSNM (mV)	370	340	382	NA	330	490	500
WSNM (mV)	335	370	335	200	360	520	590
Read Delay	120 ps	90 ps	70 ps	27 ps	NA	2.62ns	1.83 ps
Write Delay	300 ps	350 ps	1.22 ns	183 ps	1.08 ns	2.59ns	1.855ps

TABLE 2. COMPARISON TABLE

IV. CONCLUSION

The work includes the study of working of a CMOS based 7T and proposed 7T along with their different mode operations and parameter analysis. Proposed a new low power Single ended 7T SRAM cell design. Compared the parameters with conventional design, found the improvement in propagation delay FinFET based 7T.

The RSNM, WSNM, HSNM has been improved. The Write delay and the Read delay has been improved significantly to CMOS based 7T SRAM. The scope of the improvement is still vast and applicable into this proposed 7T SRAM as there is still some work to do in area of power consumption reduction and in the area of Write '0' mde operation. Hence, with scope to various parameters improvement, it is to be good to see more improvements in the proposed design

V. ACKNOWLEDGMENT

The authors would like to express sincere gratitude to Meity (Ministry of Electronics and Information Technology, Govt. of India) for providing tool support under the SMDPC2SD project and for Visvesvaraya Ph.D. Scheme.

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