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SIMULATION & CONTROL OF SFCL DEVICE WITH DC CIRCUIT BREAKER FOR FAULT CURRENT LIMITERS IN HVDC GRIDS

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Abstract— Recently, studies on HVDC circuit breaker (CB) prototypes have shown successful take a look at results. In this paper we studied the applying of resistive superconducting fault current limiters (SFCLs) on various sorts of HVDC CB so as to estimate the consequences of combining fault current limiters and conventional dc breakers. In this paper, a novel hybrid-type superconducting DCCB (D.C Circuit Breaker) model (SDCCB) is proposed. The SDCCB has a superconducting fault current limiter (SFCL) located in the main line, to limit the fault current until the final trip signal to the SDCCB is given. After the trip signal, insulated-gate bipolar transistor (IGBT) switches located in the main line will commutate the fault current into a parallel line, where dc current is forced to zero by combination of IGBTs and surge arresters. To prove the viability of the SDCCB, a simulation analysis demonstrating SDCCB current interruption performance was done for changing the intensity of dc fault current. The current limiting by the SFCL notably suppressed the dc fault current and significantly reduced the current interruption stress for SDCCB components. Matlab simulation of HVDC system with SFCL control has been done through HVDC CB.

Keywords—HVDC, SDCCB, SFCL, MTDC,etc.

I. INTRODUCTION

As we see modern civilization heavily depends on consumption of electrical energy for commercial, industrial, domestic, agricultural and social purposes. With the development of power electronics technology HVDC system based on the current source converter (CSC) and voltage source converter (VSC) has attracted widespread attention. An HVDC transmission line costs less than an AC line for the same transmission capacity. However, it is also true that HVDC terminal stations are more expensive due to the fact that they must perform the conversion from AC to DC, and DC to AC. But over a certain distance, the so called "break-even distance" (approx. 600 – 800 km), the HVDC alternative will always provide the lowest cost. Also insulation level is less compared to HVAC system.

Compared with high-voltage AC transmission, HVDC has a relatively low active power loss, while zero reactive loss. However, the impedance in a HVDC system is relatively low, when the fault occurs in a DC system, it will spread faster and wider. Therefore, fast and reliable DC circuit breakers are required to isolate faults and to minimize interference during commutation, especially when faulty lines and cables are not connected to the converter station, the fault should be cleared in milliseconds. The main component required to develop any electrical grid, whether ac or dc, is the circuit breaker that can quickly and reliably isolate the faulty network from the electrical grid. In MTDC, the dc fault current rises rapidly, and its magnitude is very large compared to that in the ac network also converters cannot operate when voltage drops below approx. 80%

II. CHALLENGES AND RESEARCH OBJECTIVES

Challenges:-

Breaking this huge dc fault current is the greatest challenge for MTDC protection system. For this reason, the main focus of HVDC CB research is on the mechanism of current zero creation across the interruption unit. So the main purpose of this topic is to study about the difference between AC and DC fault current level & getting knowledge by analysis & simulation of artificial current zero by different methods. The main objective of this thesis is to develop a new topology for HVDC circuit breaker that eliminates use of any mechanical part or MOV.

Problem Statement:-

To simulate and analyze the Hybrid HVDC circuit breaker with help of superconducting fault current limiter (SFCL) in mono-polar system.

Objectives:-
The Problem statement could be broken down to the followings objectives:

- Literature survey of HVDC circuit breakers and its operational methodology.
- Simulation of AC/DC fault current levels and its comparison.
- Simulation and analysis of different methods to make zero DC fault current.
- SFCL Implementation line and comparison between with and without SFCL in HVDC circuit breaker.
- Simulation and study of SDCCB fault current interruption by changing the values of ZSFCL and effect on fault current intensity.

III. HVDC SYSTEM

The electric power is generated, transmitted and distributed as an AC power. From the generating stations, power is transmitted to the end user via transmission and distribution lines. Transmission lines are long and operates at high or extra high voltages.

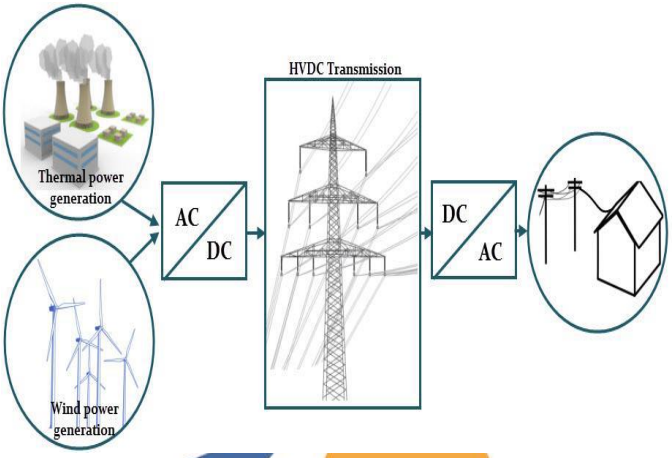

Figure 3. 1 HVDC System

At the end of the DC power system, DC power is inverted to the AC power and synchronizes with succeeding AC network. So the entire HVDC consists of three sections, namely converter station, transmission portion and an inverter station. The sending end or converter station consists of 6, 12, or 24-pulse thyristor bridge rectifier while the receiving end or inverter station consists of a similarly configured thyristor bridge but which operates in inverter mode.

Advantages of HVDC over HVAC Transmission Systems

A long distance point to point HVDC transmission scheme generally has lower overall investment cost and lower losses than an equivalent AC transmission scheme. HVDC conversion equipment at the terminal stations is costly, but the total DC transmission line costs over long distances are lower than AC line of the same distance. HVDC requires less conductor per unit distance than an AC line, as there is no need to support three phases and there is no skin effect. Depending on voltage level and construction details, HVDC transmission losses are quoted as less than 3% per 1,000 km, which are 30 – 40% less than with AC lines, at the same voltage levels. This is because direct current transfers only active power and thus causes lower losses than alternating current, which transfers both active and reactive power.

- In DC transmission, only two conductors are needed for a single line. In case of AC transmission, at least three conductors are needed and six conductors would be needed for double circuit line.
- It can transport power economically and efficiently over long distances with reduced transmission lines compared with losses in AC transmission.
- The DC link connected between two AC systems eliminates the need for maintaining the synchronization between them. The supply frequencies may or may not be equal on the two sides. HVDC systems always maintain the power flow as long as the voltage of the systems linked by HVDC is maintained at certain limits. But in case of HVAC system, synchronization of the supply frequency is must.
- The power flow in HVDC system can easily be controlled at high speed. The automatic controllers in the converter station determine the power flow through the link.
- Fault isolation between the sending end and receiving end can be dynamically achieved due to fast efficient control of the HVDC link.

Components of an HVDC Transmission System

The essential components in a HVDC transmission system are 6/12/24 pulse converters, converter transformer with suitable ratio and tap changing, filters at both DC and AC side, smoothening reactor in DC side, shunt capacitors and DC transmission lines.

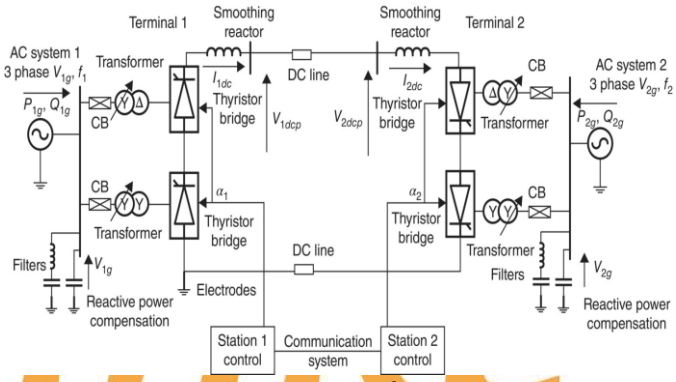

Figure 3. 2 Component of HVDC system

IV. PROPOSED WORK

Challenges:-

The main component required to develop any electrical grid, whether ac or dc, is the circuit breaker that can quickly and reliably isolate the faulty network from the electrical grid. In MTDC, the dc fault current rises rapidly, and its magnitude is very large compared to that in the ac network. Breaking this huge dc fault current is the greatest challenge for MTDC protection system [1]. Due to absence of technology to break the huge dc fault current and isolate the fault in MTDC, it is still not possible to develop MTDC, despite its numerous benefits and many practical applications. HVDC circuit breakers (DCCBs) are needed to selectively isolate a faulty line by quickly and reliably breaking the dc fault current.

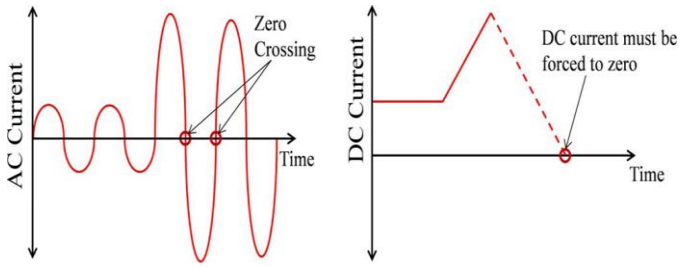

Fig. 4.1. Differences between ac and dc fault currents [1]

AC circuit breakers interrupt the ac fault current at its natural zero crossing, but there is no zero point in the dc fault current,

as shown in Fig. 4.1. Therefore, DCCBs require an active method for reducing the current to zero level before breaking the circuit. Forcing the huge and rising dc fault current to zero in HVDC systems requires methods, which are very different from conventional ac circuit breakers [1]. The three methods commonly used to make zero dc fault current are shown in Fig.4.2 and explained as follows [1]. 1) Divergent current oscillation method in which the current zero is made by magnifying the amplitude of the high-frequency oscillating dc fault current until it touches the zero point, as shown in Fig. 4.2(a). Once the current touches the zero point, an a.c circuit breaker can be used to open the circuit. This method is highly unstable because it uses large capacitors and inductors to create resonance. In addition, selection of components for its implementation depends mainly on network parameters such as line impedance and load. Therefore, a circuit breaker utilizing this method needs to be modified every time if any change in the HVDC system is made. 2) Inverse current injection method creates current zero by superimposing a high-frequency inverse current on dc fault current by discharging a pre-charged capacitor, as shown in Fig. 4.2(b).

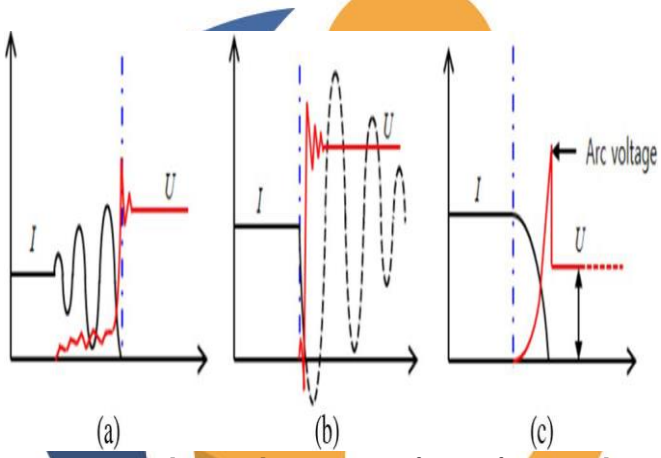

Fig. 4.2. DC voltage and current waveforms of commonly used methods for dc fault current interruption in dc switchgear. (a) Divergent current oscillation method. (b) Inverse current injection method. (c) Inverse voltage generation method [1]

This method results in a complex circuit breaker topology with large number of components and also requires an auxiliary power source to charge the capacitor. 3) Inverse voltage generating method reduces the current to zero by making the arc voltage higher than the source voltage, as shown in Fig. 4.2(c). The inverse arc voltage in the circuit breaker ignites the parallel-connected surge arresters, and the network energy is dissipated in these surge arresters, resulting in reducing the dc fault current to zero. In this paper, we investigated application studies of resistive SFCL on the various types of HVDC CB in order to estimate the effects of combining fault current limiters and conventional DC breakers. Resistive SFCL have been acknowledged as an effective solution to effectively limit fault current levels by absorbing electrical and thermal energy stresses during fault [1]. In this light, the combined application of SFCL and HVDC CB could be an attractive alternative solution capable of drastically decreasing the dissipated fault energy and improving the performance of HVDC CBs. In order to estimate the performance of combined-application of SFCL on HVDC CBs, simulation studies were performed using Matlab/Simulink. Four types of DC breakers and SFCL were modelled, and fault current interruption characteristics were compared to determine the HVDC CBs type most suitable for the application of SFCL considering the current interruption capability and reduction of total dissipated energy during DC fault.

Methodology

The proposed Superconducting D.C Circuit Breaker (SDCCB) is the combination of conventional HDCCB and SFCL. A prior-art HDCCB is shown in Fig. 3(a) and was proposed in [1]. This model works on inverse voltage generation method, as explained in this paper.

The main components of the HDCCB are shown in Fig. 3(a), and *IT* is the total current passing through the HDCCB. During normal operation, the ultrafast disconnector switch (UDS), the line commutation switch (LCS), and the residual current breaker (RCB) are closed, and they are conducting the normal dc line current. The main dc breaker (MCB) is opened, and no dc current flows through it. When a dc fault occurs, the MCB is closed, and the LCS opens. Opening the LCS commutates the current to the parallel branch containing the MCB. As the current through the LCS is decreased to a negligible value, the UDS opens with minimum arc and isolates the LCS from any voltage buildup across the HDCCB terminals.

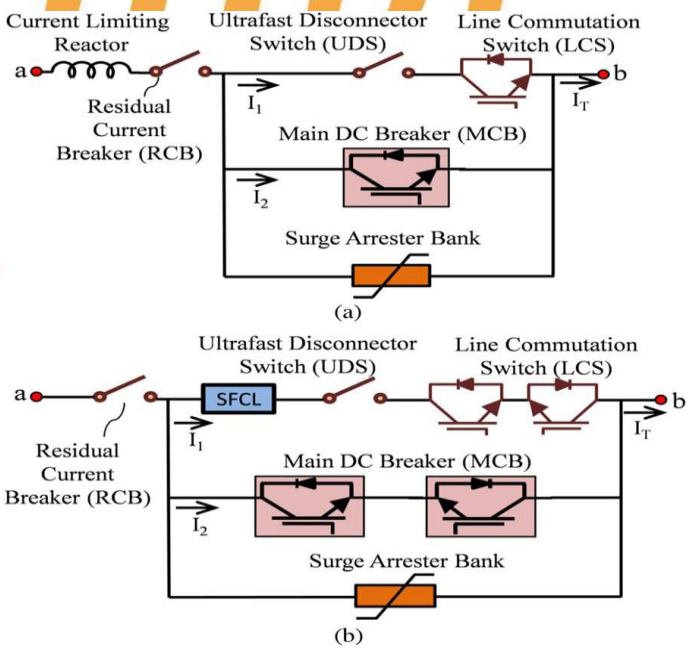

Fig. 4.3. Single-line diagram of (a) conventional HDCCB and (b) SDCCB

Once the trip signal is generated, the MCB opens, resulting in large inverse voltage buildup across the HDCCB terminals, which ignites the parallel-connected surge arrester bank and forces the dc fault current to zero. Finally, the RCB opens and isolates the HVDC line completely [1]. The HDCCB has a current-limiting reactor in series of the normal current path, as shown in Fig.4.3 (a). The current limiting in the HDCCB is done by pulse-mode operation of the MCB, by controlling the voltage drop across the current limiting reactor to zero [1].

High-power semiconductor valves, such as the MCB in Fig.

4.3(a), are composed of numerous series- and parallel-connected semiconductor switches to bear high-voltage and high-current stresses. Repeated switching of these high rated valves for current limiting may lead to their early failure due to high switching stresses [1]. Active current limiting, involving switching of large insulated-gate bipolar transistor (IGBT) valves, is the major limitation of the HDCCB. Furthermore, the presence of a series current-limiting reactor causes numerous problems. The reactor energy will be discharged during the fault, causing increased dc fault current. During the current interruption, the reactor will result in large voltage buildup across the HDCCB, due to an inductive kickback effect. In addition, larger inductance in the HVDC network will affect the dynamic response of the system during fast load shifting because of the reactor inductance, which opposes any quick change in current.

Fig. 4.3(b) shows the proposed SDCCB, which is the modified HDCCB in Fig. 4.3(a). Modifications include the following: 1) the SFCL is placed in series of the main current path (*I*1); 2) the series reactor has been removed since it is not needed anymore for current limiting; and 3) the single IGBT valve has been replaced by mirrored pair IGBT valves. The single IGBT valves in the HDCCB can only interrupt current in a single direction, i.e., from a to b in Fig. 4.3 (a). The reason for this is shown in Fig. 4.4(a), where a single IGBT, when turned off, can interrupt the current in only the forward direction, whereas a reverse current continues to flow from the IGBT antiparallel diode. Fig. 4.4(b) shows the mirrored pair configuration of IGBTs. This arrangement of IGBTs, when turned off, will break the current independent of the direction of current flow. The SDCCB does not interrupt the current instantaneously, and the decision to trip the SDCCB depends on the following: 1) eliminating the chances of a false trigger due to temporary glitches or spikes; 2) identifying the faulty line and selecting the correct DCCB among multiple DCCBs on the converter bus; or 3) crossing of safety thermal limit of any of the SDCCB components, including SFCL, LCS, and MCB. Once the trip signal is given to the SDCCB, the LCS located in the main line opens and commutates the current to the parallel line, where the dc current is made zero by combination of MCB-IGBTs and surge arresters.

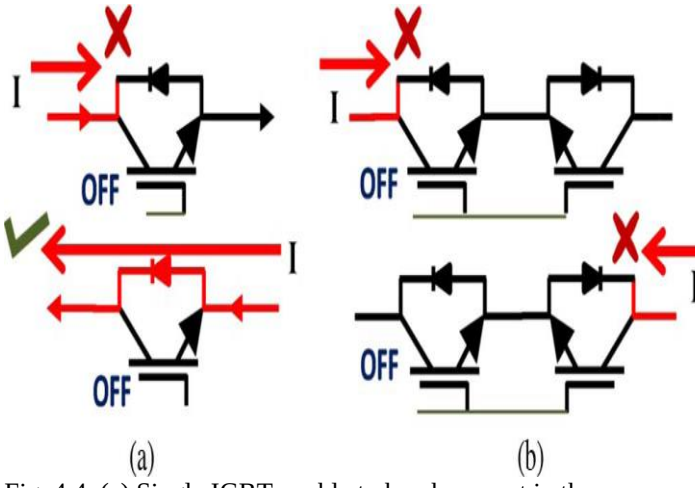

Fig. 4.4. (a) Single IGBT unable to break current in the reverse direction. (b) Mirrored pair IGBT configuration breaking current in both directions [1]

V. MODELLING AND SIMULATION

Mechanical Circuit Breaker with Help of LC Tuning

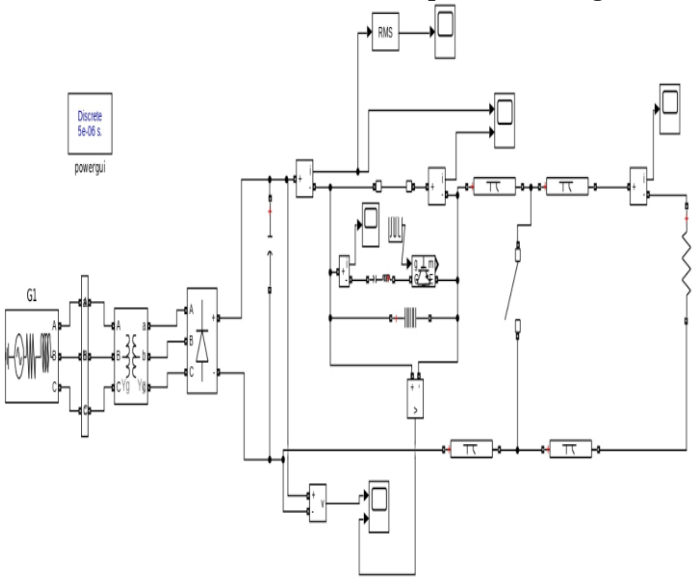

Figure 5.1 Simulation of HVDC Monopolar System with LC tuned Circuit Breaker

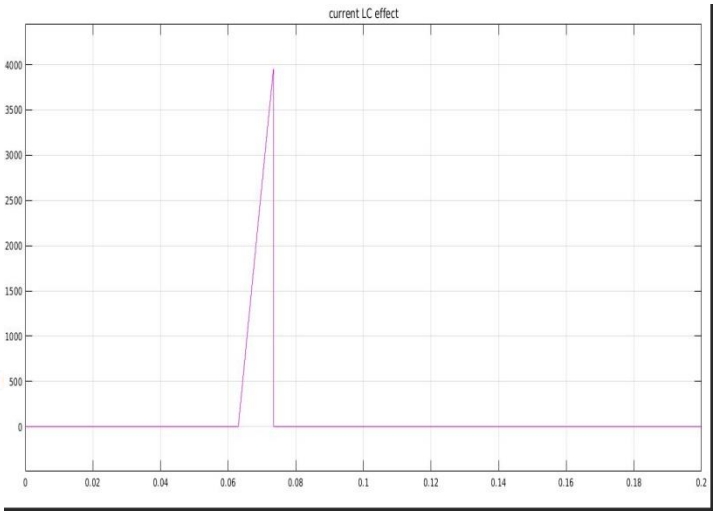

Figure 5.2 Injected Current by LC branch

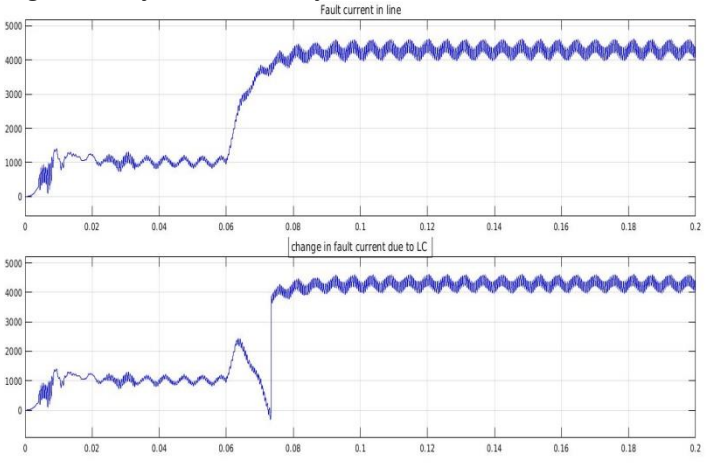

Figure 5.3 Fault current without and with effect of LC

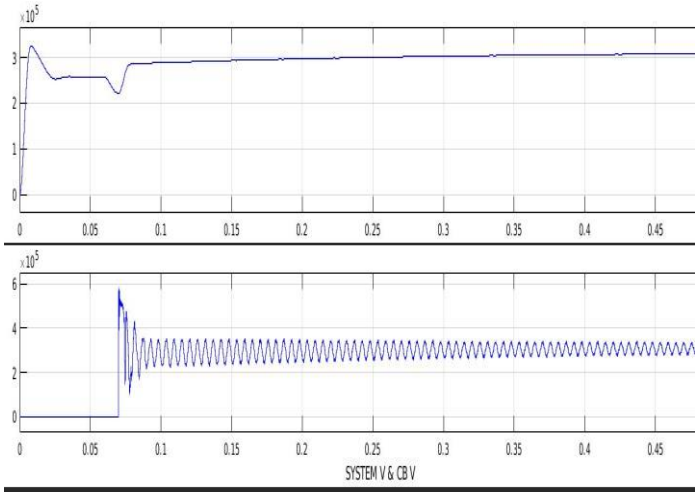

Figure 5.4 Voltage Stress across Mechanical Circuit Breaker Contact

Solid State HVDC Circuit Breaker

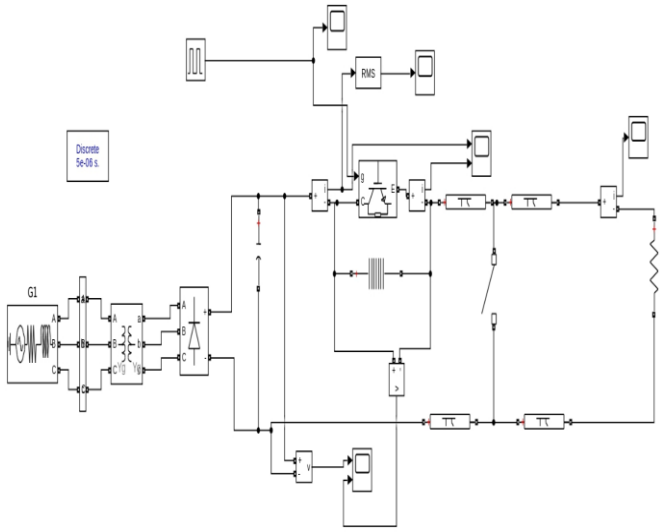

Figure 5.5 Simulation of HVDC Monopolar System with Solid State HVDC Circuit Breaker

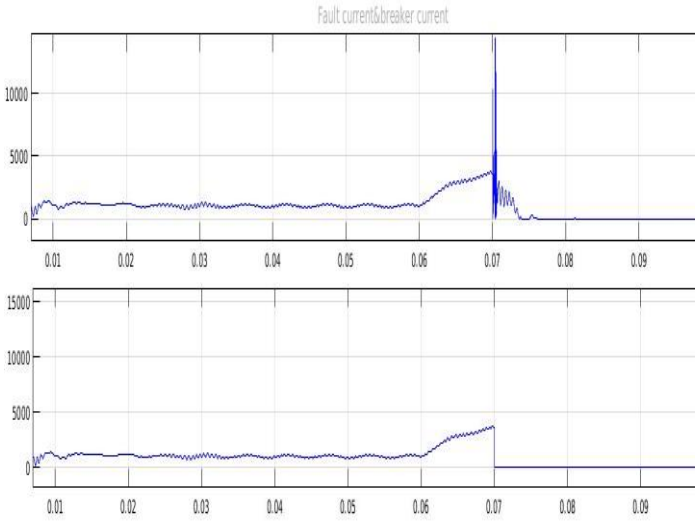

Figure 5.6 Fault current without and with solid state HVDC breaker

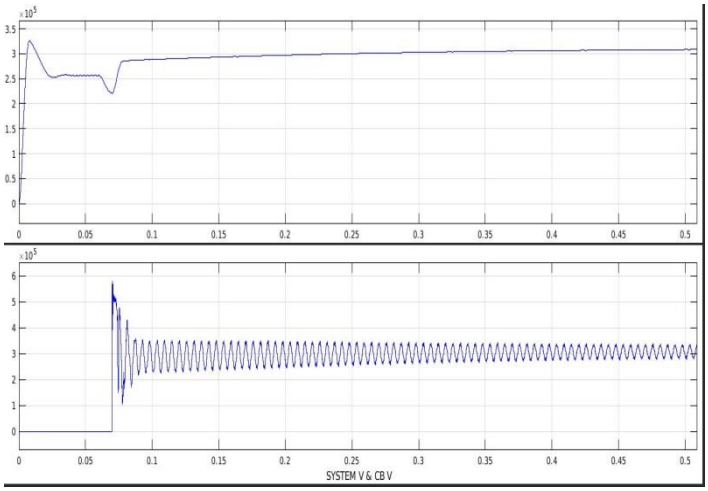

Figure 5.7 Voltage Stress across Solid State Circuit Breaker Contact

Hybrid HVDC Circuit Breaker

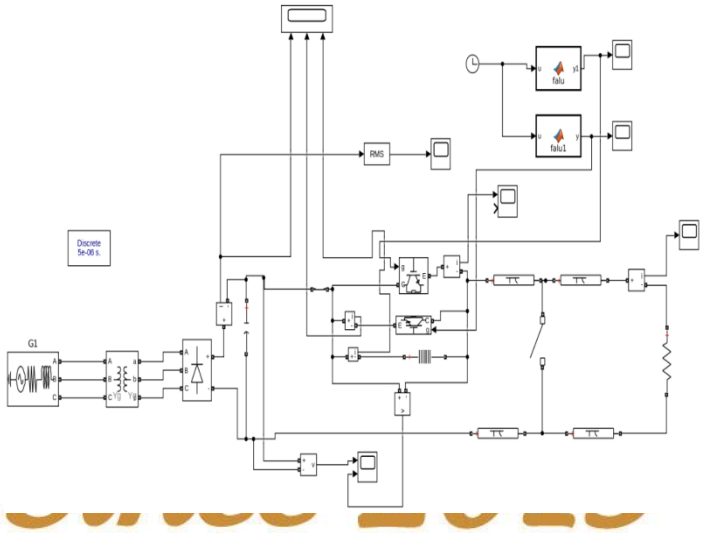

Figure 5.8 Simulation of HVDC Monopolar System with Hybrid HVDC Circuit Breaker

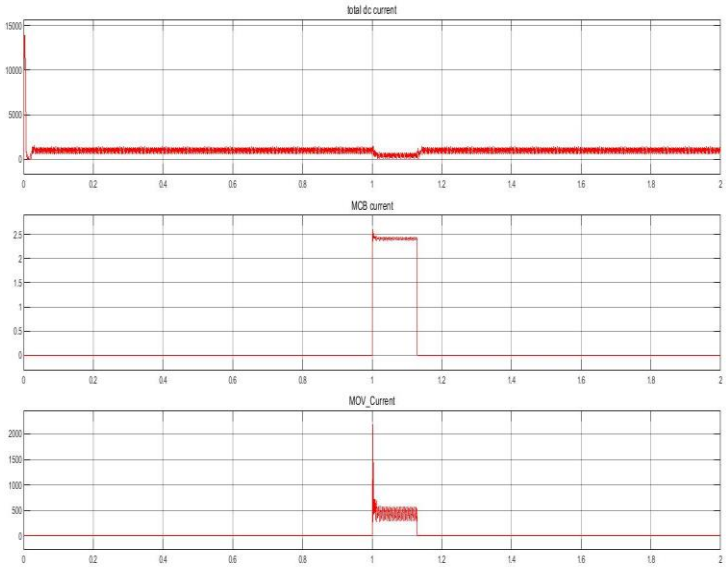

Figure 5.9 Current in Various components of Hybrid Circuit Breaker

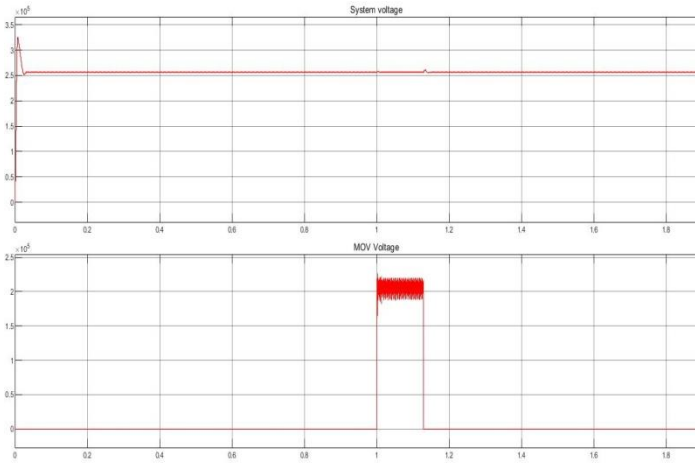

Figure 5.10 Voltage Stress across Hybrid Circuit Breaker Contact

HVDC system with proposed SDCCB System

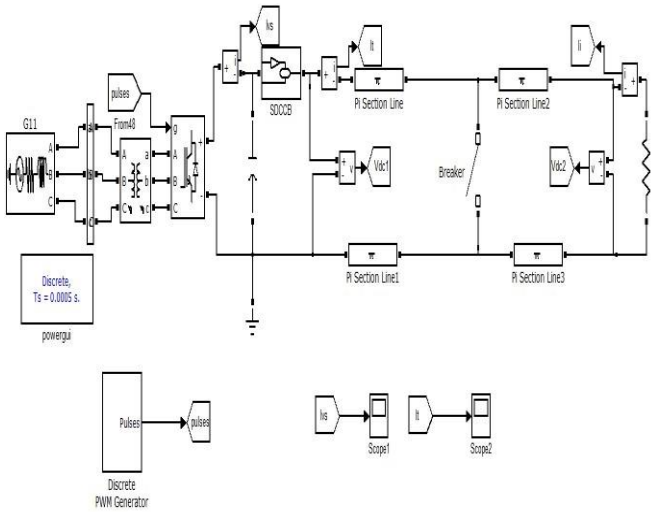

Fig 5.11- Main proposed system HVDC with SDCCB

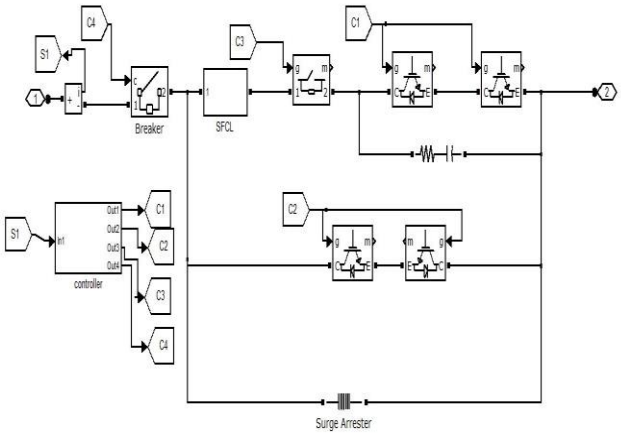

Fig 5.12- Control system of SDCCB

The main objective of SFCL in SDCCB is to suppress the increasing dc fault current to a lower level and significantly reduce the current interruption stress on SDCCB components. The SFCL will suppress the dc fault current by inserting additional impedance ZSFCL in the circuit due to its quenching. The dc fault current intensity in the test bed model is dependent on the power rating of the ac system attached with the VSC-HVDC converter station. Three categories of ac power systems are used, which are denoted as "Normal System," "Strong System," and "Very Strong System." The corresponding fault currents due to these systems are marked as In, Is, and Ivs, respectively. The type of ac systems, their power ratings, and fault current abbreviations are summarized.

Simulation Results

Fig 5.13- In with No SDCCB

Fig 5.14-Is with No SDCCB

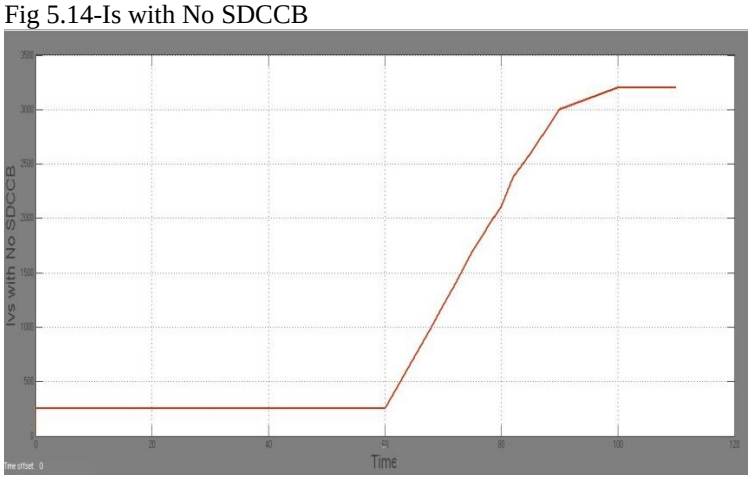

Fig 5.15-Ivs with No SDCCB

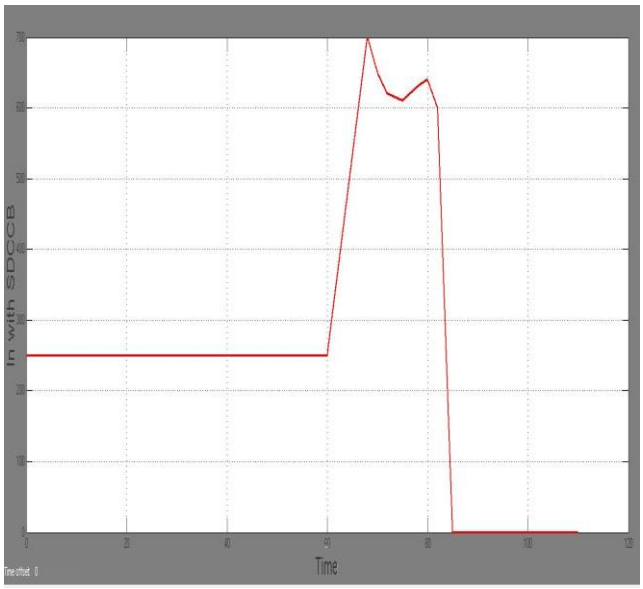

Fig 5.16- In with SDCCB

Fig 5.17- Is with SDCCB

Fig 5.18- Ivs with SDCCB

The fault current could rise to very large values if current interruption had to be delayed without current limiting, and current limiting by SFCL had significantly reduced the fault current interruption stress for other SDCCB components. Table 5.1 summarizes the percentage reduction in dc fault current, which is being interrupted after application of SDCCB. Due to the SDCCB, the dc fault current during interruption has been halved, and this will significantly decrease the ratings and size of SDCCB components. Consequently, the cost of the SDCCB would decrease. Fig. 5.19 to 5.20 shows reverse current breaking by SDCCB, when dc fault current was suddenly reversed.

Fault Current Intensity	**Total Current It with No SDCCB (kA)**	**Total Current It with SDCCB (kA)**	**Percentage Reduction in Fault current (%)**
In	**11 kA**	**6 kA**	**45.00 %**
Is	**16 kA**	**8.1 kA**	**49.40 %**
Ivs	**20 kA**	**10 kA**	**50.0 %**

Table 5.1- Percentage reduction in fault current for Changing fault current intensity

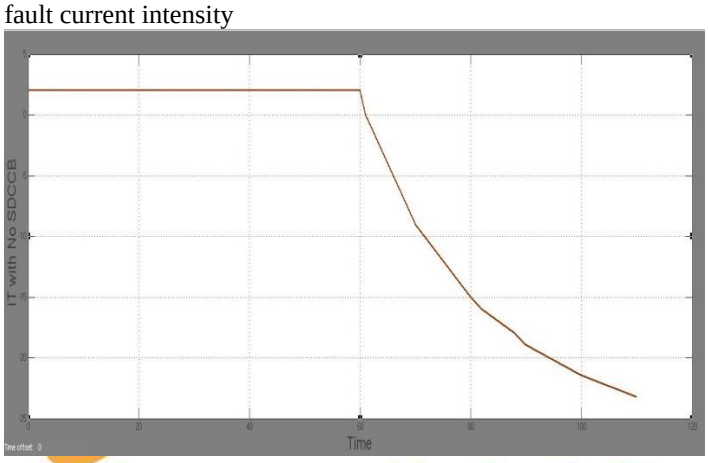

Fig 5.19- It with No SDCCB

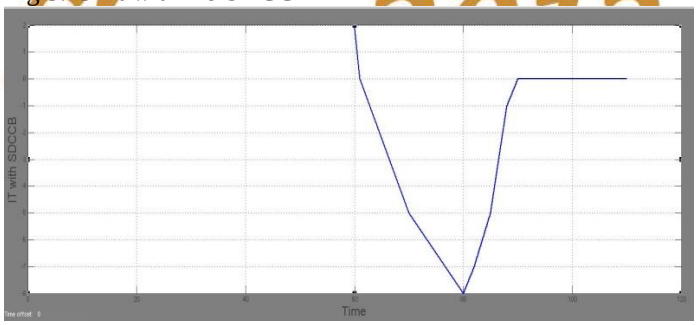

Fig 5.20 It with SDCCB

Simulation of HVDC System with MMC-Control

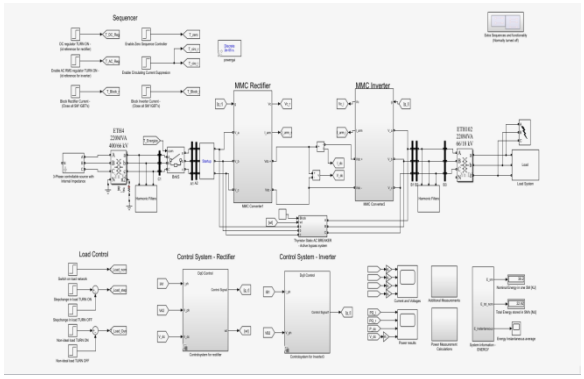

Fig 5.21- HVDC System with MMC control with SFCL

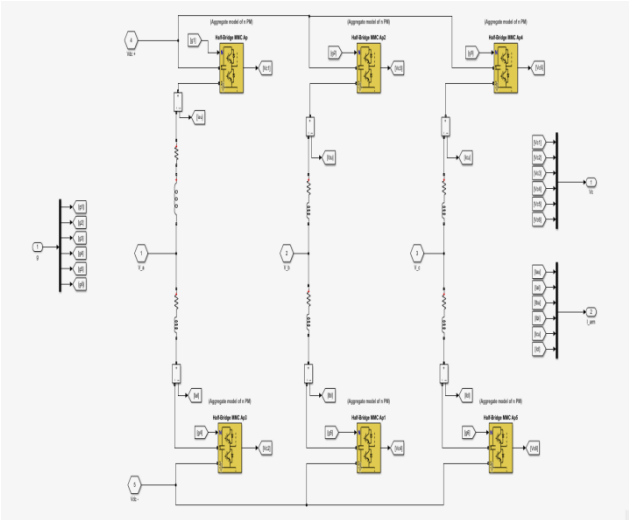

Fig 5.22-Matlab Subsystem of MMC Converter

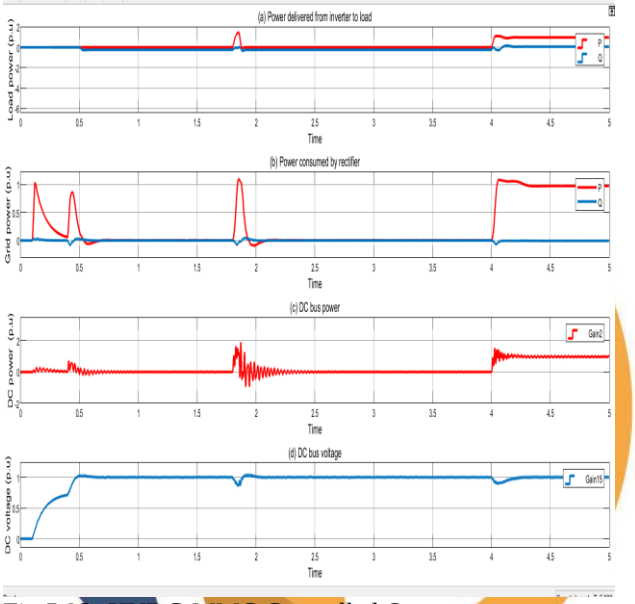

Fig 5.23- HVDC-MMC Controlled Output parameters

Fig 5.24-Fault Current variation without SFCL

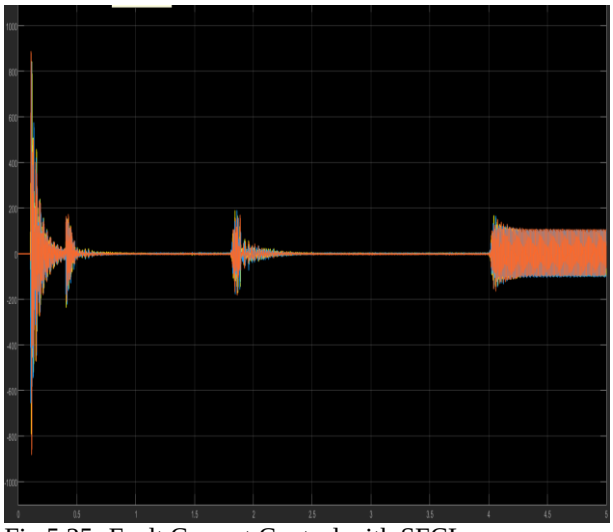

Fig 5.25- Fault Current Control with SFCL

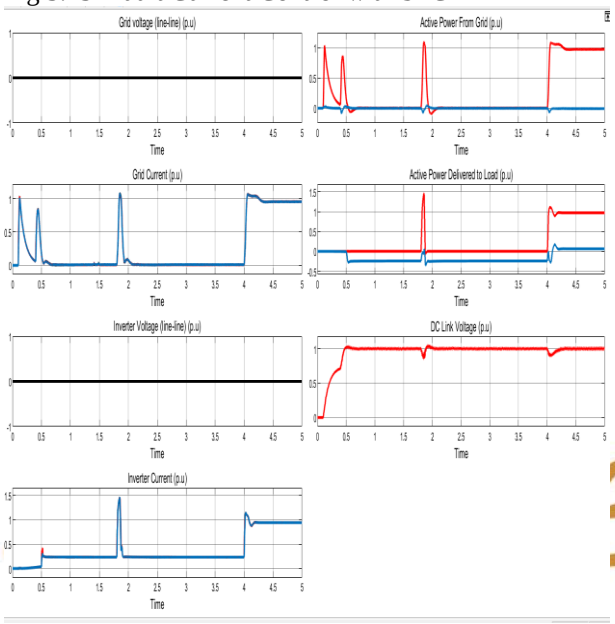

Fig 5.26- Simulation Waveform with HVDC MMC Control & SFCL use through DCCB

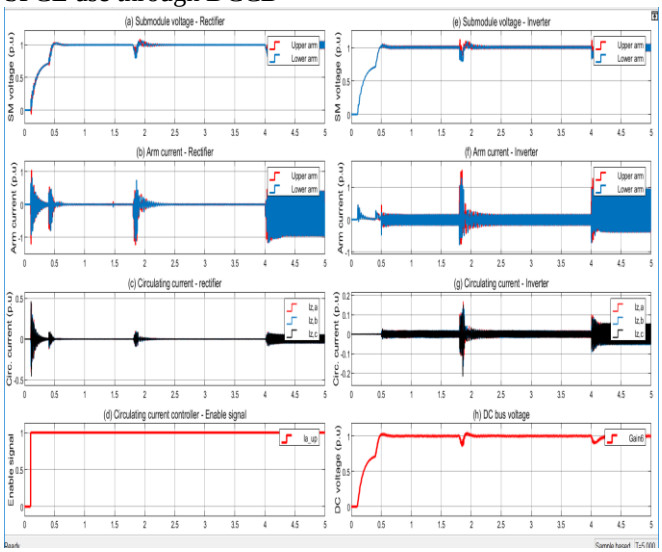

Fig 5.27- Inverter & Rectifier Side Parameter control with HVDC-MMC controlling

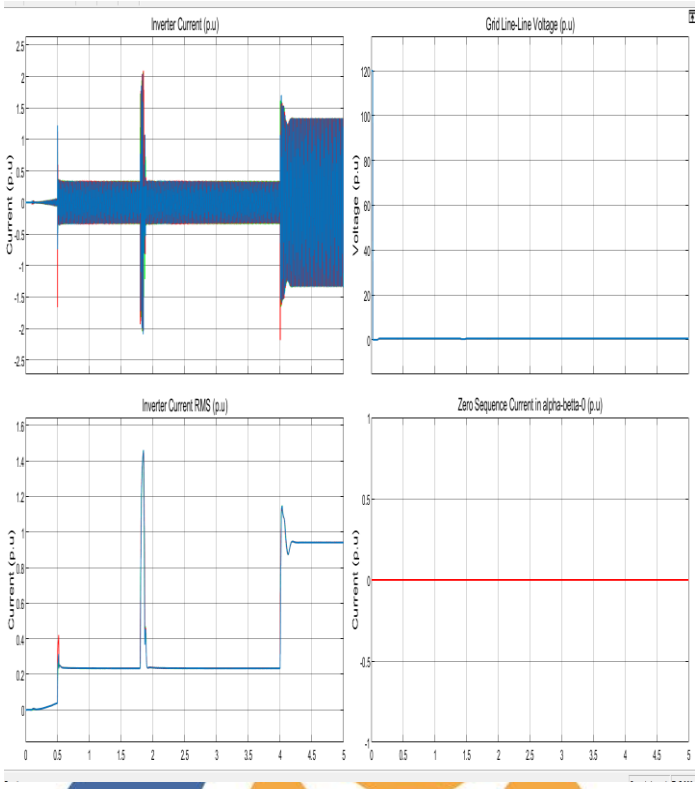

Fig 5.28-Inverter Side & Grid Side parameters control using HVDC-MMC

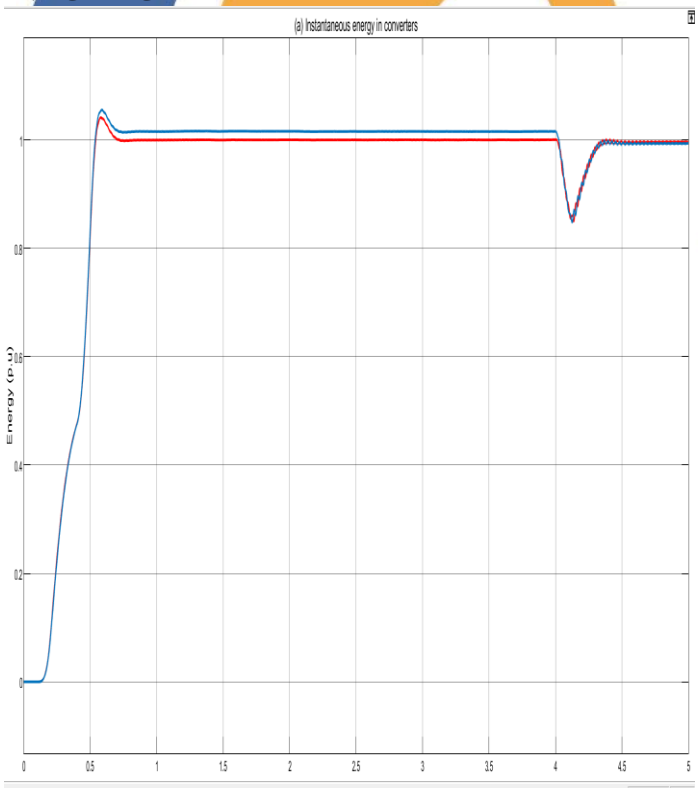

Fig 5.29- Energy dissipation control in p.u. values with HVDC-MMC control

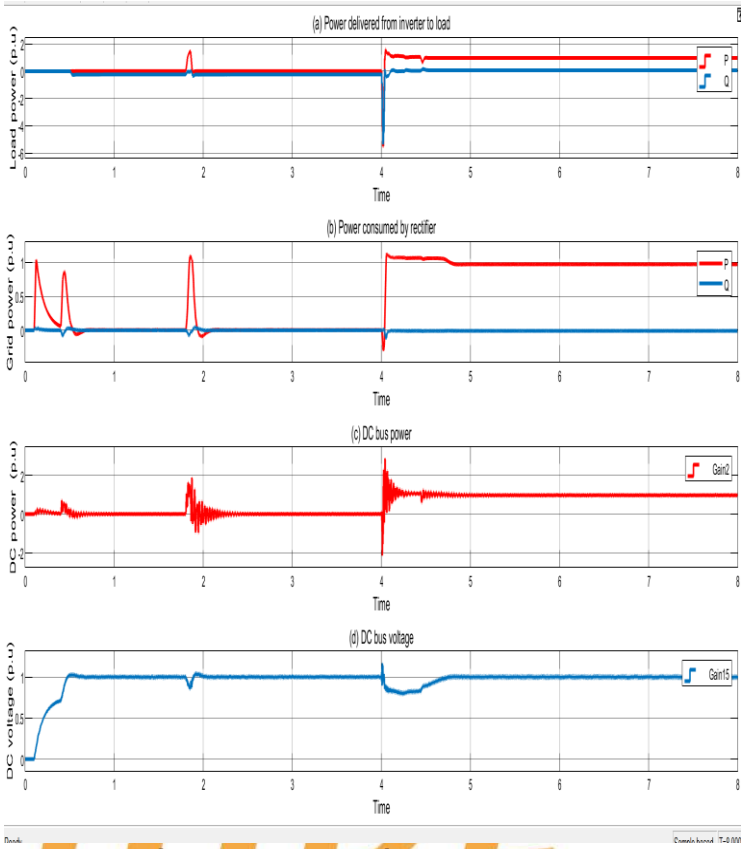

Fig 5.30-Simulation Parameters with HVDC-MMC using SFCL control

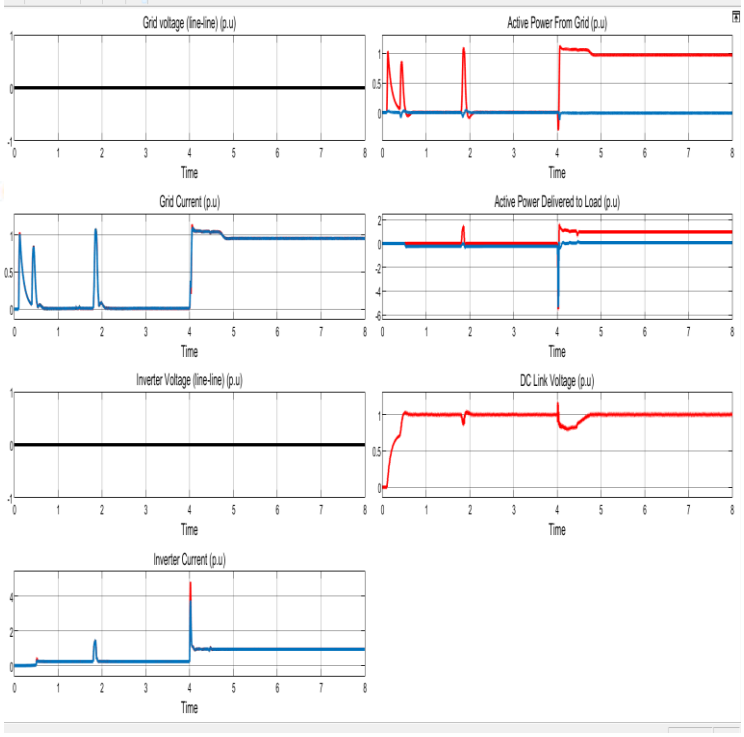

Fig 5.31- Simulation Waveform with different electrical parameters at receiving end side through MMC control

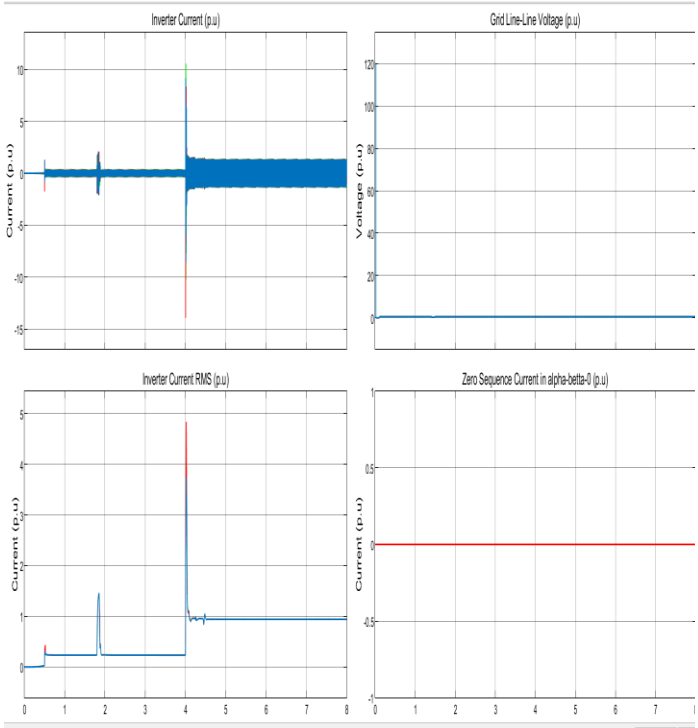

Fig 5.32- Simulation results of inverter & grid line parameters

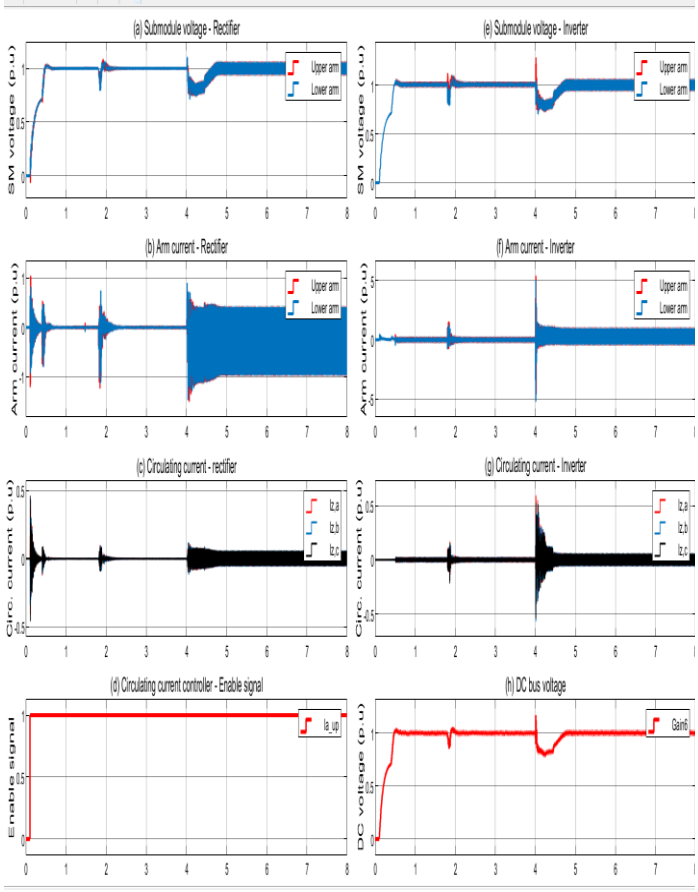

Fig 5.33- Simulation results of all parameters with SFCL & HVDC-MMC control

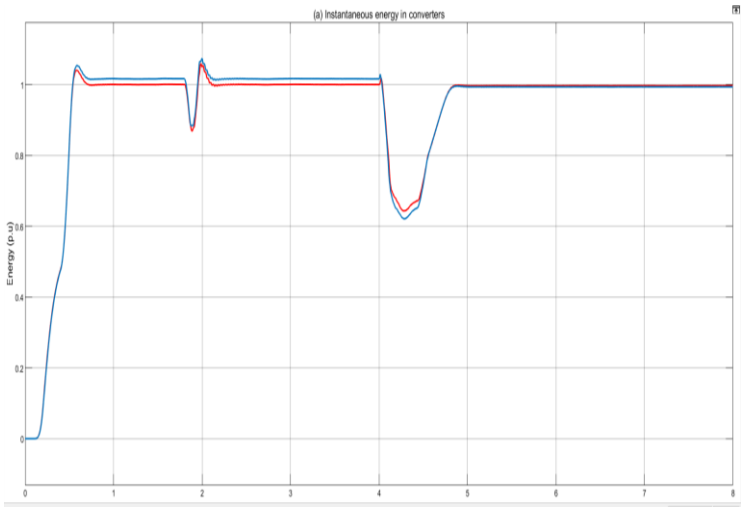

Fig 5.34- Instantaneous Energy value in p.u. with converter operation with HVDC-MMC control

SFCL Quenching Impedance Zsfcl	SDCCB Total Current It(kA)	Percentage Reduction (%)
No SFCL	20 kA	---
5 Ω	16.6 kA	19.0 %
10 Ω	13.7 kA	33.2 %
15 Ω	11.6 kA	43.4 %
20 Ω	9.9 kA	51.7 %
25 Ω	8.4 kA	59.0 %

Table 5.2- Percentage reduction in fault current for changing Zsfcl

The energy dissipated across the SFCL depends on the following:-
1) Duration of current limiting;
2) Intensity of the fault current; and
3) ZSFCL.

The current limiting time was 20 ms; the fault current intensities were In, Is, and Ivs, as shown in Table 5.2; and the ZSFCL values were selected as 5, 10, and 20 Ω. For larger ZSFCL, greater energy was dissipated across the SFCL.

Therefore, SFCL design for SDCCB is dependent on the following:
1) The selected value of ZSFCL, which determines its voltage rating and energy dissipation rating;
2) The maximum value of the prospective fault current in the HVDC network, which depends on the strength of the integrated ac system and the complexity of the MTDC; and
3) The maximum time that the SFCL must limit the fault current in the SDCCB before the trip signal.

VI. CONCLUSION

This paper proposes a novel protection scheme for HVDC transmission lines. This paper has explored the simulation of

AC/DC fault current levels and its comparison. Simulation and analysis of different methods to make zero DC fault current. From the simulation results, interruption time, and dissipated energy stress on an HVDC CB could be decreased by using Hybrid HVDC CB. Noticeable enhancement of the fault interruption capability was exhibited by PRCB, which showed the longest interruption time and highest maximum fault current. Solid state HVDC circuit breaker having high conduction losses. So by simulation results it should be proved that HDCCB overcomes the limitations of mechanical CB as well as solid state CB. We have proposed a novel hybrid-type SDCCB, in which a conventional HDCCB is combined with the SFCL. Working principles of the proposed SDCCB were explained, followed by a simulation analysis demonstrating the SDCCB current interruption ability for changing the intensity of dc fault current. The current limiting by the SFCL notably suppressed the dc fault current and significantly reduced the current interruption stress for SDCCB components. Furthermore fundamental design requirements for SFCL in SDCCB were investigated, including the effect of SFCL quenching impedance on the SFCL voltage rating and energy dissipation capacity.

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