REVIEW PAPER ON LOW POWER SHIFT REGISTER IN CMOS TECHNOLOGY

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Abstract: ***In modern VLSI design, reducing power consumption has become a primary objective due to the increasing demand for portable and battery-operated electronic devices. Shift registers, being fundamental components in digital systems such as communication, signal processing, and memory units, contribute significantly to overall power dissipation. Conventional CMOS-based shift registers suffer from high dynamic and leakage power, especially in deep submicron technologies. This review paper focuses on low-power design techniques for shift registers using CMOS technology, with particular emphasis on the Zigzag technique and the Sleepy Keeper approach. The Zigzag technique aims to reduce dynamic power by minimizing switching activity and eliminating unnecessary transitions in the circuit. It improves efficiency during active operation by controlling internal node behavior. On the other hand, the Sleepy Keeper approach targets leakage power reduction by incorporating sleep transistors and keeper circuits, which maintain logic state during standby mode while significantly reducing leakage current. This paper presents a comparative analysis of both techniques in terms of power consumption, performance, and implementation complexity. Furthermore, it highlights the advantages of integrating both methods to achieve optimized power efficiency in both active and idle states. The study concludes that a hybrid approach combining Zigzag and Sleepy Keeper techniques provides an effective solution for designing low-power shift registers in advanced CMOS technologies, making it suitable for energy-efficient VLSI applications.***

Keywords: Low Power VLSI, CMOS Technology, Shift Register, Zigzag Technique, Sleepy Keeper, Leakage Power Reduction, VLSI Circuits

I. INTRODUCTION

With the rapid advancement of semiconductor technology, VLSI systems have become increasingly complex and powerful. Modern electronic devices such as smartphones, wearable gadgets, and Internet of Things (IoT) systems demand high performance while operating under strict power constraints. As a result, low-power design has emerged as a critical requirement in digital circuit design, particularly in CMOS technology, which is widely used due to its high noise immunity and low static power consumption. However, as technology scales down into deep submicron regions, power dissipation—especially leakage power—has become a significant challenge for designers [1].

Among the various components of digital systems, shift registers play a vital role in data storage, transfer, and synchronization. A shift register is a sequential circuit composed of a chain of flip-flops, where the output of one flip-flop is connected to the input of the next. These circuits are extensively used in applications such as digital signal processing, communication systems, image processing, and memory units. Despite their simplicity, shift registers contribute considerably to overall power consumption due to continuous clock switching and frequent data transitions. Therefore, optimizing shift register design is essential for achieving energy-efficient VLSI systems [2, 3].

Power dissipation in CMOS circuits is broadly classified into dynamic power and static (leakage) power. Dynamic power is caused by the charging and discharging of load capacitances during switching activity, while leakage power arises due to sub-threshold currents, gate oxide leakage, and reverse bias junction leakage. In earlier technologies, dynamic power dominated; however, in modern nanometer-scale technologies, leakage power has become equally significant. Consequently, there is a growing need for design techniques that can effectively reduce both dynamic and leakage power components without compromising performance [4].

Several techniques have been proposed in the literature to address power reduction in shift registers. These include clock gating, pulse-triggered flip-flops, dual-edge triggered designs, and various logic restructuring methods. Among these, the Zigzag technique and the Sleepy Keeper approach have gained considerable attention due to their effectiveness in targeting different aspects of power consumption. The Zigzag technique focuses on reducing dynamic power by minimizing switching activity and eliminating unnecessary transitions in the circuit. It achieves this by modifying the internal structure of logic gates and controlling signal propagation paths, thereby reducing glitching and redundant operations. This makes it particularly useful during active operation when the circuit is frequently switching [5, 6].

On the other hand, the Sleepy Keeper approach is a leakage reduction technique designed to minimize static power consumption during idle or standby modes. It introduces additional sleep transistors along with keeper transistors that help retain the logic state even when the circuit is partially turned off. Unlike conventional power gating techniques that may lead to data loss, the Sleepy Keeper method ensures state retention while significantly reducing leakage currents. This makes it highly suitable for applications where circuits spend a considerable amount of time in standby mode.

The integration of these two techniques offers a promising solution for designing low-power shift registers. While the Zigzag technique enhances efficiency during active operation by reducing switching power, the Sleepy Keeper approach ensures minimal leakage during idle periods. Together, they provide a balanced approach to power optimization across different operating conditions [7].

This review paper aims to provide a comprehensive study of low-power shift register design in CMOS technology, focusing on the Zigzag and Sleepy Keeper techniques. It analyzes their working principles, advantages, limitations, and performance trade-offs. Furthermore, it explores the potential benefits of combining these approaches to achieve optimal power efficiency. The insights presented in this paper are expected to aid researchers and designers in developing advanced low-power VLSI systems suitable for next-generation electronic applications.

II. LITERATURE REVIEW

G. D. B and J. R (2025) presented a detailed study on the design and analysis of low-power level shifters in CMOS technology, focusing on minimizing power dissipation while maintaining signal integrity across different voltage domains. Their work emphasizes the importance of efficient voltage level conversion in modern low-power systems, where multiple supply voltages are used to optimize energy consumption. The authors proposed optimized transistor sizing and circuit techniques to reduce both dynamic and leakage power. Their analysis shows that careful design of level shifters can significantly improve overall system efficiency, which is highly relevant for shift register circuits that often operate across different voltage levels in integrated systems.

G. C. Reddy et al. (2023) proposed a low-power unidirectional shift register design aimed at reducing power consumption and improving operational efficiency. The authors utilized optimized flip-flop structures and minimized clock transitions to reduce dynamic power dissipation. Their implementation demonstrated that by reducing unnecessary switching activity and improving data flow direction, significant power savings could be achieved. The study also highlighted the importance of clock management techniques, which directly influence the performance of shift registers in communication and signal processing applications.

B. R. Kumar et al. (2025) introduced a low-power True Single Phase Clock (TSPC) flip-flop integrated with auto-gated clock gating and power gating techniques. Their approach effectively reduces both dynamic and static power consumption by disabling the clock signal during inactive periods and cutting off leakage paths. The proposed design showed improved energy efficiency and reduced delay compared to conventional flip-flops. This work is particularly important for shift register design, as flip-flops are the core components, and any improvement at this level directly enhances overall system performance.

C. J. Prakash et al. (2025) explored the design of a 4-bit shift register using 18nm FinFET technology and hybrid logic flip-flops. Their research demonstrated that FinFET-based designs offer better control over short-channel effects and significantly reduce leakage power compared to traditional CMOS technology. The hybrid logic approach further enhanced performance by optimizing switching characteristics. The results indicated improved speed, reduced power consumption, and better scalability, making it suitable for next-generation low-power VLSI systems.

M. Gholamnia Roshan and M. Gholami (2024) proposed universal shift registers using Quantum-dot Cellular Automata (QCA) technology, focusing on achieving low latency and high efficiency. Their design eliminates the need for conventional transistors and instead relies on quantum interactions for data transfer. The study demonstrated that QCA-based shift registers offer extremely low power consumption and high-speed operation, making them a promising alternative for future nanoscale circuit design.

C. R. K. Reddy et al. (2023) developed a low-power Serial Peripheral Interface (SPI) shift register with improved energy efficiency and reduced hardware complexity. Their design focused on optimizing data transmission and minimizing switching activity within the register. The results showed a significant reduction in power consumption while maintaining reliable communication performance. This work is particularly relevant for embedded systems where SPI-based communication is widely used.

Y. Cai et al. (2020) proposed an ultra-low power 18-transistor fully static flip-flop in 65nm CMOS technology. Their design achieved substantial reduction in leakage power while maintaining robustness and stability. The use of a fully static structure ensured reliable operation even at low supply voltages. This work highlights the importance of efficient flip-flop design in reducing overall power consumption in sequential circuits such as shift registers.

D. Blaauw and D. Sylvester (2020) provided a comprehensive overview of near-threshold voltage design techniques for low-power circuits. Their work discussed various strategies for reducing power consumption by operating circuits near the threshold voltage, where energy efficiency is maximized. However, challenges such as increased delay and variability were also addressed. These techniques are highly applicable to shift register design, especially in ultra-low power applications.

M. T. I. Badal et al. (2020) presented a low-power shift register design using pulse-triggered flip-flops. Their approach reduced

clock power by generating narrow pulses instead of continuous clock signals, thereby minimizing switching activity. The design demonstrated improved power efficiency and reduced transistor count compared to conventional shift registers, making it suitable for high-performance and low-power applications.

Sai Srinivas Chandra et al. (2023) investigated secure CMOS logic design using logic encryption techniques. Their work focused on enhancing hardware security while maintaining low power consumption. Although primarily aimed at security, the proposed techniques also contribute to efficient logic design by optimizing circuit structure and reducing unnecessary transitions. This research provides additional insights into designing robust and power-efficient CMOS-based systems, including shift registers.

III. ZIGZAG AND SLEEPY KEEPER TECHNIQUES

In low-power VLSI design, reducing both dynamic and leakage power is essential for improving overall system efficiency. Among various techniques, the Zigzag technique and the Sleepy Keeper approach have emerged as effective solutions targeting different components of power dissipation in CMOS circuits. These techniques are particularly useful in the design of shift registers, where continuous switching and idle-state leakage significantly contribute to power consumption.

A. Zigzag Technique

The Zigzag technique is primarily used to reduce dynamic power consumption in CMOS circuits by minimizing switching activity. Dynamic power is directly proportional to the switching frequency and capacitive load; therefore, reducing unnecessary transitions plays a crucial role in power optimization. The Zigzag approach modifies the internal structure of logic circuits in such a way that signal transitions follow an optimized path, thereby avoiding redundant switching and glitch generation.

In this technique, transistors are arranged in a “zigzag” manner, which helps in controlling the flow of signals and reducing the number of active switching nodes at any given time. This leads to a reduction in short-circuit currents and dynamic power dissipation. Additionally, the Zigzag structure improves signal stability by limiting unwanted transitions, which further enhances circuit reliability.

One of the key advantages of the Zigzag technique is that it does not require additional control signals or complex circuitry, making it relatively simple to implement. It is highly effective during active operation when the circuit experiences frequent switching. However, its limitation lies in the fact that it does not significantly address leakage power, which becomes dominant in deep submicron technologies.

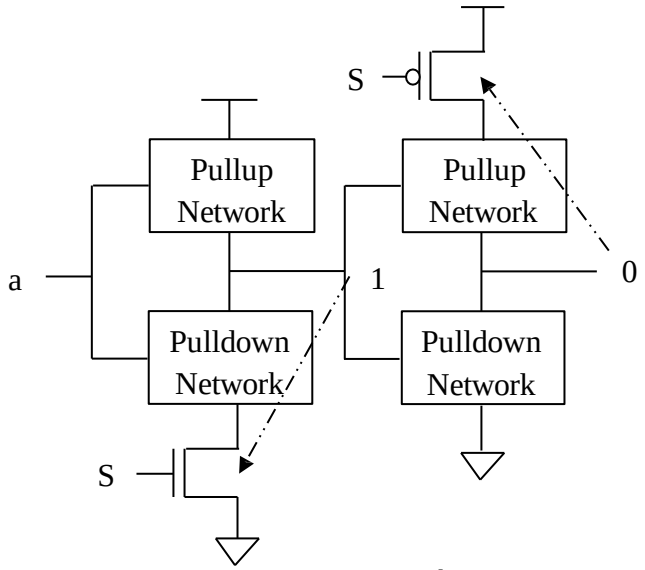

Figure 1: Zigzag Technique

B. Sleepy Keeper Technique

The Sleepy Keeper technique is a leakage power reduction method designed to minimize static power consumption in CMOS circuits during standby or idle modes. With the scaling of technology, leakage currents such as sub-threshold leakage and gate oxide leakage have become major contributors to total power dissipation. The Sleepy Keeper approach effectively addresses this issue by incorporating sleep transistors along with keeper transistors in the circuit design.

In this technique, additional PMOS and NMOS sleep transistors are inserted between the power supply (Vdd) and ground

(GND). During active mode, these transistors remain ON, allowing normal circuit operation. During standby mode, they are turned OFF, effectively cutting off the leakage paths and reducing static power consumption. Meanwhile, keeper transistors are used to maintain the logic state of the circuit, preventing data loss that typically occurs in conventional power gating techniques.

The major advantage of the Sleepy Keeper technique is its ability to significantly reduce leakage power while preserving data integrity. This makes it highly suitable for applications where circuits spend a considerable amount of time in idle mode. However, it introduces additional hardware overhead and slightly increases circuit complexity and area.

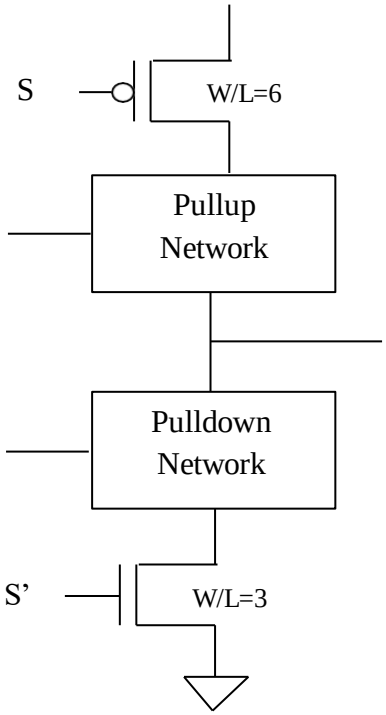

Figure 2**:** Sleepy Keeper Technique

IV. SHIFT REGISTER

A shift register is a sequential digital circuit widely used for data storage and data transfer in digital systems. It is constructed using a series of flip-flops connected in cascade, where each flip-flop stores one bit of information. All the flip-flops are driven by a common clock signal, ensuring synchronized operation. The basic function of a shift register is to shift data from one flip-flop to the next with each clock pulse. When a clock signal is applied, the data present at the input of the first flip-flop is transferred to its output, and simultaneously, the data from each stage moves to the next stage in sequence. In this way, binary data is shifted either to the left or right depending on the design configuration.

For example, in a 4-bit shift register, four D flip-flops are connected in series. The serial input is applied to the first flip-flop, and its output is connected to the input of the second flip-flop, and so on. With every clock pulse, the input data propagates through the chain, and the final output is obtained from the last flip-flop. This type of arrangement is known as a Serial-In Serial-Out (SISO) shift register. Other configurations such as Serial-In Parallel-Out (SIPO), Parallel-In Serial-Out (PISO), and Parallel-In Parallel-Out (PIPO) are also used depending on application requirements.

Shift registers are essential components in many digital applications, including communication systems, signal processing, and memory units. However, due to continuous clocking and frequent switching activity, they consume a significant amount of power in CMOS technology. Therefore, optimizing shift register design using low-power techniques such as Zigzag and Sleepy Keeper is important for improving overall system efficiency in modern VLSI applications.

V. METHODOLOGY

The methodology focuses on designing a low-power shift register in CMOS technology by integrating both the Zigzag technique and the Sleepy Keeper approach. The objective is to reduce dynamic power during active mode and leakage power during standby mode, thereby achieving overall energy-efficient performance.

Initially, a conventional shift register is designed using D flip-flops, which form the basic storage elements. Each flip-flop is connected in cascade to enable data shifting with every clock pulse. To reduce dynamic power, the Zigzag technique is applied by modifying the internal structure of the logic gates within the flip-flops. This arrangement minimizes unnecessary switching activity and avoids glitching, which significantly reduces dynamic power consumption during data transitions.

Next, the Sleepy Keeper technique is incorporated into the design to address leakage power. In this approach, sleep transistors (PMOS near Vdd and NMOS near GND) are added to control the power supply during idle conditions. Additionally, keeper transistors are used to retain the logic state when the circuit is in sleep mode. During active operation, sleep transistors remain ON, allowing normal functioning. During standby mode, they are turned OFF to cut leakage paths, while keeper transistors maintain data integrity.

The combined implementation ensures that the shift register operates efficiently in both active and idle states. Simulation and performance analysis are then carried out to evaluate improvements in power consumption, delay, and area compared to conventional designs.

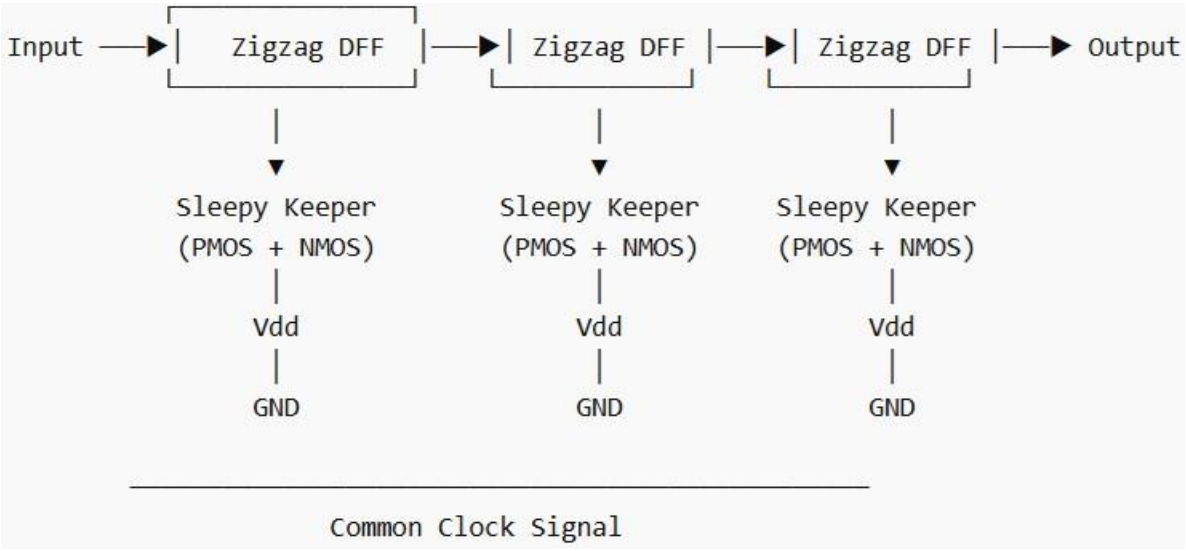

Figure 3: Shift Register using Zigzag and Sleepy Keeper technique

VI. CONCLUSION

This review paper presents a comprehensive analysis of low-power shift register design using CMOS technology, with a specific focus on the Zigzag technique and the Sleepy Keeper approach. As power consumption continues to be a major concern in modern VLSI systems, especially in portable and battery-operated devices, efficient design methodologies are essential to achieve optimal performance and energy efficiency.

The study highlights that conventional shift registers consume significant dynamic and leakage power due to continuous clock switching and scaling effects in deep submicron technologies. The Zigzag technique effectively addresses dynamic power reduction by minimizing switching activity and eliminating unnecessary transitions within the circuit. It proves to be highly beneficial during active operation, improving overall performance with moderate design complexity.

In contrast, the Sleepy Keeper approach focuses on reducing leakage power by incorporating sleep transistors and keeper circuits. It ensures state retention during standby mode while significantly lowering leakage currents, making it suitable for low-power and idle-state applications. Although it introduces additional hardware overhead, the power savings achieved outweigh the increase in area and complexity.

Furthermore, the combined use of Zigzag and Sleepy Keeper techniques offers a balanced and efficient solution for both active and idle modes of operation. This hybrid approach results in substantial power reduction, improved reliability, and enhanced performance of shift registers. Future research can explore the implementation of these techniques in emerging technologies such as FinFET and CNTFET to further enhance low-power VLSI design.

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